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HIGH VOLTAGE SOLAR ARRAY CONFIGURATION STUDY

By

B. G. Herron, D. E. Creed, R. W. Opjorden and G. T. Todd

HUGHES AIRCRAFT COMPANY

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FINAL REPORT

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By

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FOREWORD

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ABSTRACT

A detailed conceptual design study of high voltage solar arrays with integral power conditioning, capable of providing high voltage regulated power (15 kw, 1 to 16 kv) to multiple loads has been performed. The major areas considered are: 1) solar array power subdivision, 2) regulation, 3) power transfer and reconfiguration, 4) components for mechanization, 5) array performance, and 6) questions related to high voltage design, fabrication, and testing. The general conclusions are that high voltage arrays are feasible and that they can out-perform conventional power conditioning systems operated from low voltage arrays. The results are applicable to most space missions utilizing solar electric power.

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1. INTRODUCTION AND SUMMARY

There is currently a strong interest in space missions using ion thruster systems and high power communication systems. Both of these loads would require conditioned high voltage power. The physical and operational properties of the two systems are analogous; hence, it would be desirable to develop power sources which would be compatible with either load and which would allow the power to be shared or transferred between loads in multiphase missions.

This study investigates concepts of providing the required conditioned power through high voltage solar arrays with integral power conditioning. This approach promises simplicity of design, high long term reliability, and a lower system specific weight penalty than could be accomplished with conventional power conditioning operated from a low voltage array.

An example mission application in which a high power communication satellite would be raised from low earth orbit to synchronous orbit with ion thrusters was used to give early direction to the study. In this application the array power, 15 kw (end-of-life) at voltage levels between 1 and 16 kv, would be transferred from the orbit raising propulsion system to high power communication tubes upon reaching synchronous altitude. Although the example mission has unified the study it has not curtailed the generality of the results. The findings of the study are applicable to a myriad of space missions requiring conditioned power which would be derived from a solar electric source.

The major objective of this study was to investigate conceptual electrical configurations to determine the preferred design approaches and the required components which would lead to reliable systems with low weight and area penalties. This has required consideration of solar array power subdivision, regulation techniques, and power transfer and protection circuitry. The high voltage design principles established in the High Voltage Solar Array Study (Reference 1) were used to support design of the arrays in this study.

The system concept envisioned for the high voltage solar array with integral power conditioning is shown in Figure 1. Blocks of solar cell power, regulation switches, clamp switches, reconfiguration switches, and blocking or power steering diodes comprise the array.

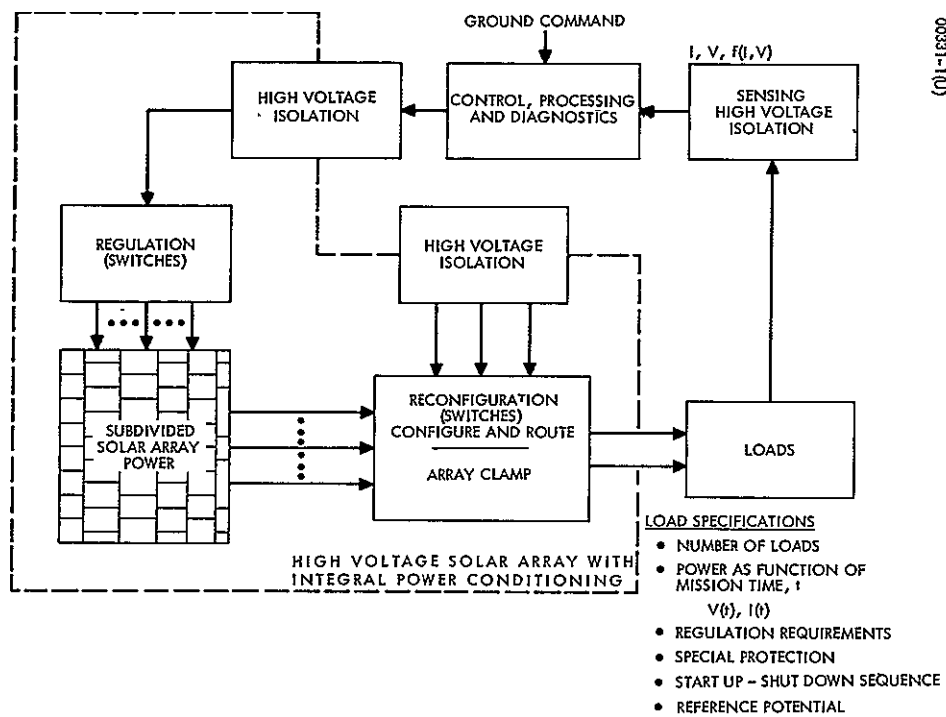


Figure 1. System Concept

Specific system design is guided by the load specifications. The array power would be subdivided into power blocks sized in voltage and current ratings to satisfy the load specification. These blocks would be combined and routed to the appropriate using loads via the reconfiguration switches. Regulation of the outputs (to compensate for load variation and source variations due to thermal, particulate radiation, and plasma environmental aspects) would be achieved by modifying the load power I-V characteristics in discrete increments with regulation switches. In general, each output would be composed of many power blocks connected in series, parallel, or series-parallel combinations. Not all of the blocks would contain regulation switches. A regulation accuracy of ± 0.1 percent is possible with a comparable sensor accuracy. Closed-loop regulation would be mechanized via sensors and on-board logic.

The clamp switches would function as an on-off control for individual power blocks. These switches would perform dynamic protection tasks and would allow reconfiguration to occur without current flow in the reconfiguration switches under sunlit conditions. In addition, the clamp switches can be used in combination with load sensing to verify reconfiguration on a block-by-block basis before applying full power to the load.

The control signals for all of the above switches would emanate from on-board control, processing, and diagnostic logic. The logic decides, on the basis of its design format and sensed data, the states that should be assumed by the individual switches. Intermediate drive logic (which derives its bias power from adjacent solar cells) can be placed with the regulation switches. This approach reduces the number of high voltage interfaces.

High voltage isolation is required to transmit switch control signals and to receive sensed data from points referenced at high voltage with respect to the control logic. Photon-coupled transmission is considered the preferred means of achieving this isolation.

The data sensed at high voltage can be voltage, current, or other load parameters which are influenced by the voltage or current levels. The sensed data will generally be analog; hence, a sensor which performs an analog-to-digital conversion in a form compatible with the control logic appears desirable when bridging the high voltage. This digital technique would eliminate sensor error due to variation in isolation coupling efficiency.

The results of the study indicate that the above system concept, and other similar concepts, can be taken to hardware development with present technology. Once the few major components are developed, each new power system design for high voltage power would involve little more than minor modifications in the location of these components and simple changes in the low level logic formats which control the switches.

In the solar array sections of this report, two approaches will be suggested for the conceptual design of a high voltage array. The first involves optimization of the array design to a specific mission. The second

is universal in concept and basically independent of mission. The specific concept has the advantage of high load matching efficiency, while the universal concept offers greater flexibility with mission changes.

A model will be suggested and configured for each of the two conceptual approaches. Both will be developed in sufficient detail to allow the calculation of performance increments. These increments are defined as weight and area changes for specific high voltage design actions, changes in relationship to a contract defined, conventional low voltage array (Reference 2).

Two models have been chosen, rather than one, to allow the development of performance increment boundaries. The specific model is optimistic, the universal model is more pessimistic. These boundaries should bracket the actual performance of a final design. They should also give a feeling for the penalties involved in the universal approach.

Both arrays configured are models. A final design would probably lie between the two models in concept and performance. A judgment will be made delineating the most fruitful area of future design effort for high voltage arrays. The method suggested involves computer optimization of the array layout for specific missions. This approach to large area array design promises high array efficiency, second-order mission flexibility, and a logical method of parametric tradeoffs.

The primary performance increment penalty in the array area will be the minimum required thickness of the substrate and coverslide for high voltage design. A method involving the use of conductive coatings will be suggested to overcome this thickness barrier. Performance increments will be presented with and without such coatings for both array models.

Two areas will be shown that heavily influence the final choice of an optimum conceptual design. These are fabrication and test. Past studies in large area arrays have emphasized the conceptual design of multikilowatt arrays. However, only several hundred-watt arrays have been fabricated and tested to demonstrate feasibility.

The results of this study support the key design decision made in respect to the solar panel in the first High Voltage Array Study (Reference 1):

Any practical low voltage array can be designed to operate at high voltage with only a minimum of modification.

The methods for such design are proposed. The best use of such arrays will require full mission analysis and tradeoffs.

The regulation section (Section 4) presents designs and the design considerations for achieving accurate constant voltage and constant current regulation. The relationships between load and source variance and regulation range are illustrated in a design example. Desirable characteristics of

switches to accomplish the regulation are given, and techniques for accomplishing the necessary sensing are discussed. The logic requirements for single loop and multiloop regulation control are presented. Finally, the problems related to the placement of electronic on the panel are discussed.

Weight penalty estimates for regulation of the array models will be shown to range between 0.25 kg/kw (0.6 lb/kw) and 0.45 kg/kw (1 lb/kw). The regulation of electrical power efficiency should be between 99 and 100 percent at end-of-life.

The reconfiguration section (Section 5) presents a number of conceptual reconfiguration switching arrangements that would allow the power-load interconnects to be changed. These switching arrangements are discussed in terms of critical failure modes and the number of switches required for mechanization with a given number of power blocks and using loads. The requirements for clamping the array and for blocking devices are discussed and related to the total system operation.

Desirable electrical characteristics for reconfiguration switches are given and the interrelationship of block voltage sizing, switch voltage drops, and array power efficiency are established.

The candidate switches for mechanizing the switching arrangements are reviewed and operational and development problems are discussed. Array control modes including the logic of operation for reconfiguration, dynamic protection, start-up, shutdown, and high voltage clamping are discussed for two systems. One system uses mechanical reconfiguration switches, the other solid-state switches.

For the two array models configured in this study, the estimated weight penalties for reconfiguration and control (less regulation) ranged between 0.41 kg/kw (0.9 lb/kw) and 1.36 kg/kw (3 lb/kw). For power blocks above 500 volts the power transfer efficiency should exceed 98 percent.

It appears possible to develop high voltage arrays with only minor modifications to existing devices; however, it is recommended that the few required critical components defined in this study be specifically developed for this application. Such development would optimize array performance and reliability. The two major problem areas requiring such development are high voltage isolation for control and sensing and electronic packaging to handle the environmental extremes.

2. SOLAR ARRAY CONCEPTUAL ANALYSIS

2.1 INTRODUCTION

The purpose of the solar array sections of this report is to develop array models allowing calculation of performance increments. The performance increments are defined as weight and area changes for a high voltage array compared with conventional low voltage arrays.

Two array models will be developed in some detail. One will allow an optimistic comparison with conventional arrays, the other more pessimistic. Such an approach permits boundaries to be established for the performance increments. As a result, it may be assumed that the most probable array lies between the two bounds. The two models are termed the universal concept and specific concept. The universal concept is a design independent of mission, while the specific concept is optimized in design to a specific mission. As expected, the universal concept exhibits higher flexibility in respect to mission changes and lower efficiency in matching actual mission loads.

The effects of one major perturbation on the two models will also be shown. This is the design action of employing a conductive coating on the coverglass face as well as on the back of the substrate. If such a coating were developed, it would allow minimization of the major weight penalties for high voltage in the array design. These penalties are due to the increased coverslide and dielectric substrate thicknesses required to stand off the charge buildup on the array under plasma environment (Reference 1).

The initial discussions of the two models will be conceptual in nature. More detailed layout will be developed in the next section. Terminology employed in the solar array discussions is listed in Table 1.

2.1.1 Conclusions

Two array concepts, the universal and specific, will be configured to establish upper and lower bounds for a realistic performance estimate of high voltage arrays.

TABLE 1. SOLAR ARRAY TERMINOLOGY

Performance increment	The change in power per unit weight and unit area for a high voltage array compared with a conventional low voltage array. The increments are based on specific actions for high voltage design.
Universal concept	Array with configuration basically independent of mission.
Universal model	Array chosen to represent the universal concept.
Specific concept	Array optimized to meet a specific mission.
Specific model	Array chosen to represent the specific concept.
Boundary	Either the optimistic or pessimistic sum performance increment. Represented by the specific model and universal model, respectively.
Solar cell	Smallest electrical producing element. Single crystal silicon element.
Group	Basic solar cell assembly. Building block of series/parallel connected cells.
Bypass module	The set of cells wired in parallel with a diode for the purpose of failure isolation, primarily open circuit failure.
Sector	A limited number of groups of solar cells connected in series. The limit is generally the largest unit tested prior to final assembly.
Panel segment	The basic fabrication unit for the specific model, full panel width by one sector, with eight sectors attached. Eleven panel segments are joined together to form a panel as the final step in assembly.
Block	The basic I-V assembly for providing power to the spacecraft loads. Reconfiguration and regulation is accomplished through operation on the blocks.

Table 1 (continued)

Division	The nine blocks on the universal array which must be connected in parallel to yield full current capability, 14 cells in parallel, for a given 500 or 1000 volt increment.
Panel	One of four physical entities of the power producing configuration. It is approximately 4.6 meters (15 feet) by 25.9 meters (85 feet) in area.
Array	Four panels, the full power configuration, approximate total of 985,600 solar cells.

2.2 CONCEPTUAL MODELS

Since the contract established a base low voltage array for high voltage-low voltage comparison which is a four panel flexible array, this study will assume a four panel array.

2.2.1 The Universal Concept

The assumptions made in developing a universal model are threefold. First, there will be no layout changes required for any specific mission. Second, all configuring will be accomplished by hard-wiring and switches located in a configuration section at the base of the panel. Finally, all four panels of the array are identical.

A total of 180 blocks of power have been chosen for the universal array. The blocks with their respective current and voltage levels are shown in Figure 2. The total number of blocks represent four identical panels with 45 blocks on each panel.

To provide course load voltage matching to within ± 250 volts for six simultaneous loads, eight 500-volt divisions are required. One 500-volt division per load is the minimum necessary. It is clear that each load must receive a course voltage level which is greater than or equal to the desired regulated level; hence, the maximum voltage mismatch would be less than 500 volts. To configure four identical panels, the number of divisions at each voltage level must be divisible by four. A division is the full current capability for a given voltage level. In the present case, nine blocks are in parallel per division. Fourteen cells in parallel are required to satisfy end-of-life power requirements for the suggested orbit raising mission.

Course load current matching to within ± 0.5 the current output of a 2×2 cm solar cell ± 0.34 ampere end-of-life, is accomplished through the use of five single-cell strings, three two-cell strings, and one three-cell string in each voltage division (see Figure 2). This configuration provides

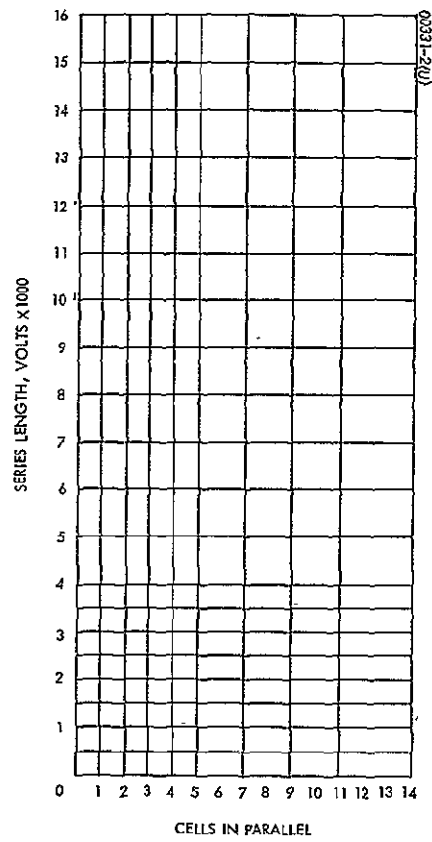


Figure 2. Cell Block Schematic,
Universal Approach

course signal cell current precision for five of the six loads. The last can use any of the remaining current. This approach allows stacking of blocks in various parallel and series combinations. Fine current regulation is provided by closed-loop modification of the I-V characteristics of the configured load power. This is discussed later in Section 4.

In summary, a full current range is available for each voltage division, 500 volts and 1000 volts. In addition, any and all loads can require 500 volt blocks simultaneously.

This conceptual array will serve as the universal array model to be configured in detail in Section 3. One of the four identical panels is shown in Figure 3.

2.2.2 The Specific Concept

Three basic criteria are assumed in conceiving the specific array model. First, panel layout is adapted to each mission. Second, in reconfiguration, switching is employed only for load sequencing and to provide redundancy of blocks. Finally, the individual panels need not be identical in the most general sense. Rather, the array and each individual panel are optimized for the given mission.

In general, this optimization takes the form of a statistical computer program. The developed software will take into account the requirements for actual loads, load sequencing, and reliability/redundancy requirements. Initial work has been done in the development of such software. The efforts in this area will be described in the next section.

For the purpose of establishing the optimistic bound for a high voltage array compared with low voltage, a simplified specific array model will be assumed and configured. Figure 4 shows one of four identical panels of the array. Identical panels are assumed for the sake of simplicity; however, the panels of the specific array need not be identical. In choosing this panel for the specific model, it will be assumed that the six simultaneous loads can be covered by a total of sixteen 1-kv blocks, end-of-life. Each block has a full complement of 14 cells in parallel to provide 0.94 ampere end-of-life. There is no subdivision of the current levels through the use of smaller current blocks.

The above assumptions, in terms of mission, allow the development of an optimistic bound for the calculation of performance increments. Although such a simplification is being made, the methods of computer optimization of a more complex specific array will be shown.

2.2.3 Conclusions

Two models for the high voltage array have been conceived. Both concepts will be configured to allow the establishment of an optimistic and a more pessimistic boundary for the establishment of performance increments.

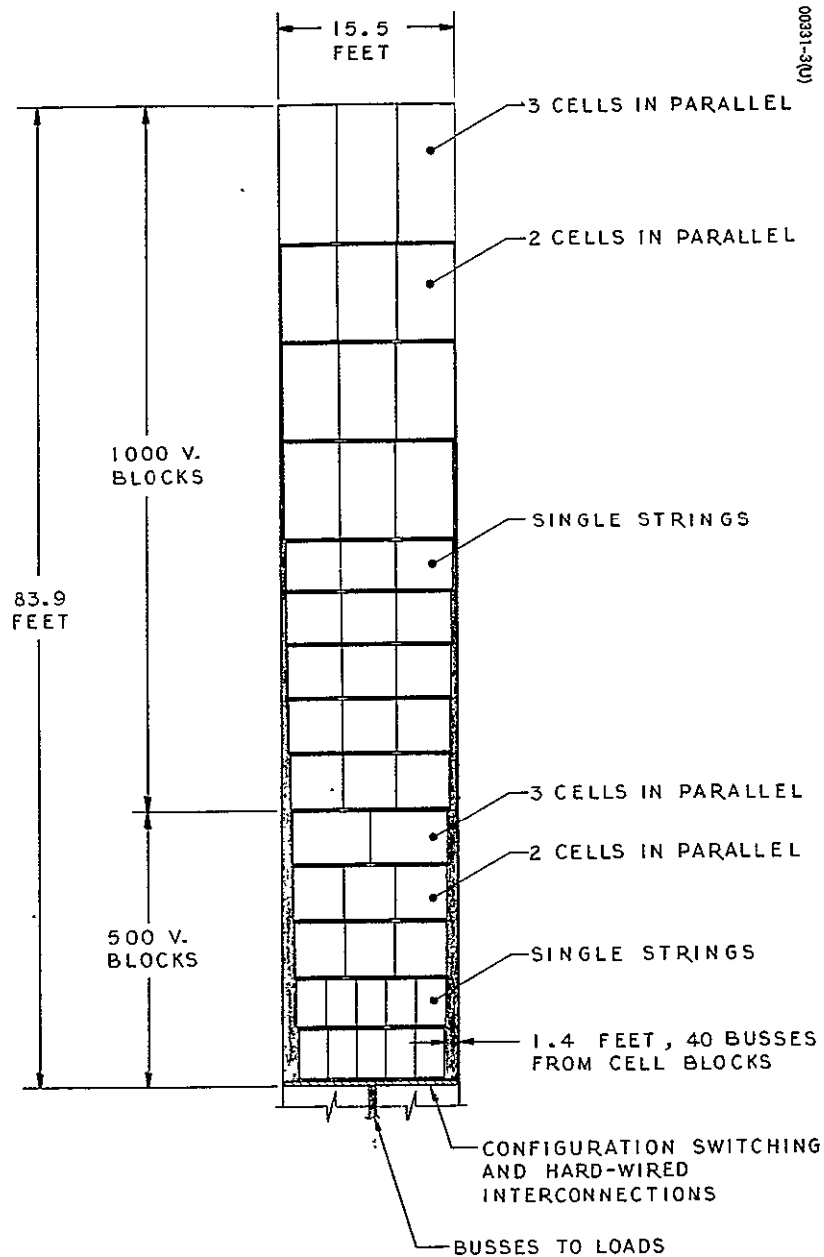


Figure 3. Solar Cell Block Layout, Universal Approach

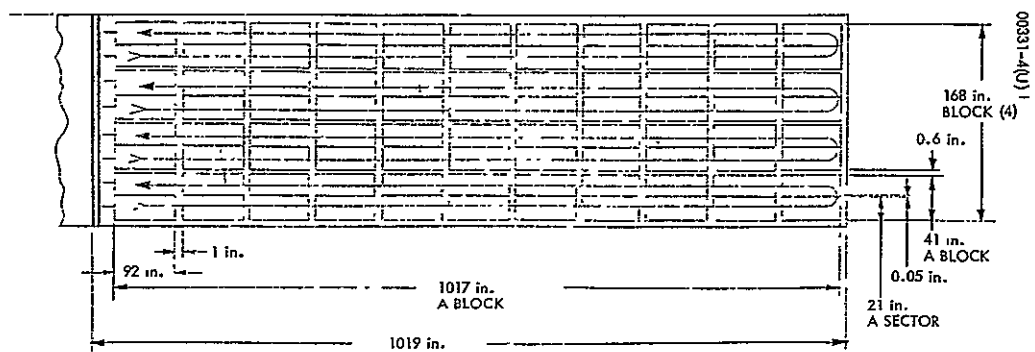
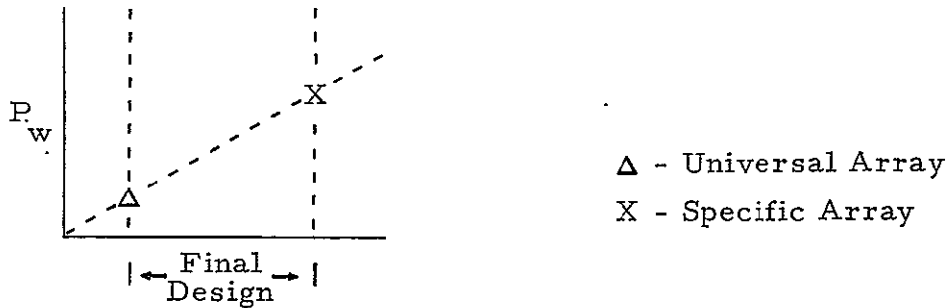


Figure 4. Solar Cell Block Layout, Specific Approach



2.3 COMPARISON OF CONCEPTUAL MODELS

If it is assumed that both models fulfill the minimum required reliability and load sequencing capability, the basis for comparison of the models becomes twofold. First, the models are judged in terms of flexibility with respect to mission variations. Second, the efficiency in terms of matching the loads must be considered. Efficiency, in turn, impacts on weight and area. In array design, inefficiency must be compensated for by additional power.

On the basis of the twofold criteria for conceptual comparison, the universal model shows higher flexibility but lower efficiency. The 180 block universal model has an efficiency of 94 percent in matching the loads. An optimized specific model of 180 blocks would have an approximate efficiency of 97 percent. The 97 percent figure is considered pessimistic; refinement of existing software should increase efficiency for the specific concept.

Although the specific concept has lower flexibility, this is a first order effect. Once the software is developed for model optimization by computer, the specific concept has high second order flexibility. Layout changes would be minimal for a change in missions. Hard-wiring and switching would be changed from mission to mission.

Certain other advantages exist for the specific concept. It can be configured with less border area, fewer buses and leads, fewer switches, and power for a given load from fewer panels.

2.3.1 Conclusions

The universal concept has higher first order flexibility. At the same time, the specific concept allows higher efficiency in matching the loads. Both concepts will be configured in the form of the proposed conceptual models.

3. SOLAR ARRAY DESIGN AND CONFIGURATION

3.1 INTRODUCTION

The two array models chosen to represent the universal and specific concepts will be configured in this section. Design will be entered in sufficient detail to allow performance estimates to be made for both arrays.

Array design and configuration will be divided into two portions. First, the elements common to both the universal and specific models will be discussed. Second, each model will be configured in its uniqueness.

A primary penalty in terms of weight for high voltage operation is increased thickness of the coverslide and flexible substrate. Such thickness increases, compared to low voltage arrays, are considered necessary to stand off charge buildup due to high voltage operation in a plasma environment. An alternate action will be proposed which could eliminate this penalty. The alternate action is the use of conductive coatings (Reference 1) The performance increments at the end of this report will be calculated both with and without such coatings for the array models.

A final summary will evaluate the two models and their use in performance prediction. In addition, comments about the projected design for a high voltage array will be given. A technique for array optimization through computer software will be suggested. Initial work on such software has been accomplished.

3.2 COMPONENTS AND ACTIONS COMMON TO BOTH MODELS

The items presented below are common to both the universal and specific models.

3.2.1 Components and Materials

Solar Cell/Coverslide Selection

A summary of the solar cell types and parameters considered under this study is presented in Table 2. Because of the rather severe radiation environment for the orbit-raising mission, 10 ohm-cm base resistivity

TABLE 2. TYPES OF SOLAR CELLS—HIGH VOLTAGE, FLEXIBLE ARRAY

Cell Type	Advantages	Disadvantages	Comments
Silicon N/P — boron doped	Extensively tested and flown		
Base resistivity			
2 ohm-cm	Higher voltage at maximum power point in mild radiation environment	Maximum power degrades more rapidly than 10 ohm-cm under radiation	Employ 10 ohm-cm at greater than 5×10^{15} electrons/cm ² (1 mev) total fluence
10 ohm-cm	Higher current		This mission requires 10 ohm-cm
Thickness			
Increase	Higher efficiency	Advantages of thickness disappears after 10^{15} electrons/cm ² (1 mev)	
Decrease		Very fragile — increased costs. Knee tends to soften under radiation. Backside radiation effects increase	
Silicon P/N — boron doped		Severe radiation effects	No advantage — this mission
Silicon N/P — lithium doped	Apparent annealing of radiation damage	Insufficient and inconclusive test results	Questions unresolved. 1) Does recovery occur under <u>continuous</u> radiation in vacuum? 2) What is the rate of redegradation?
			The highest efficiency cells may not be the best annealing.
Thin film — cadmium sulfide	Weight savings, radiation resistance, applicability to flexible arrays, low cost	Adverse environmental effects; low efficiency	Not acceptable at present but status may change with new manufacturing techniques
New cell types			
Thin film — cadmium sulfide		Requires additional development and testing	
Cu ₂ Se, GaAs, poly-crystalline silicon		Low efficiency — requires additional development and testing	Eliminated from consideration
Multifunction cells		Rapid degradation under radiation	

N/P silicon cells were chosen. Some consideration was given to lithium doped rather than boron doped cells. However, as is outlined in Table 2, uncertainty as to the ability to consistently anneal radiation damage effects in lithium doped cells led to the choice of boron doped cells. If annealing is chosen as a method of compensation for radiation degradation, boron doped cells are preferred at present. Cadmium sulfide cells are not

acceptable at this time, but their status might change prior to the building of a high voltage array through the development of new cell manufacturing techniques.

The basic issue in terms of solar cell/coverslide choice for the high voltage array is the determination of cell and coverslide thickness. This parameter will have the greatest effect on performance increment calculations. Figure 5 presents the trend of weight/unit power as a function of cell/coverslide combinations of equivalent thickness. The trend includes the effects of substrate area variations, as well as thickness changes. It is noted that weight/unit power continues to decrease with decreasing cell/coverslide thickness, even though mission radiation degradation effects have been included. The trend represents end-of-life conditions. Such a trend would seem to indicate a principle of the thinner the better. However, the optimum thickness is impacted by three factors.

First, thickness of the cell and coverslide should be equal to optimize protection from radiation degradation. For an array configured on thin flexible substrates, backside as well as front side particulate damage must be considered. Based on limited testing at Hughes, it may be assumed that an equal thickness cell and coverslide, together with the suggested Kapton substrate for the high voltage array, will provide equal protection on the front side and backside. Both the Kapton substrate and the cell thickness to the junction region provide backside protection. Additional testing is now in progress to further assess backside radiation effects on cells mounted on thin flexible substrates. It should be stressed that backside effects must be included in performance predictions for flexible substrates. Based on the above assumption of equivalent thickness, the pacing item in the selection of the cell thickness becomes the minimum required coverslide thickness. If the cell were thinner than the coverslide, backside radiation effects would nullify any advantage due to the thicker coverslide.

Therefore the second, and pacing, item leading to the choice of thicknesses is the coverslide thickness necessary to withstand charge buildup in the plasma environment. The dielectric strength of the quartz coverslide is shown in Figure 6. Performance predictions for the high voltage array indicate that beginning-of-life open circuit voltage will be approximately 30 kv. This value represents maximum array voltage. If it is assumed that maximum voltage could be seen only during communication, without ion engines on, the array will be floating in respect to the plasma. At maximum beginning-of-life voltage, under these conditions, voltage gradients on the dielectric surfaces of the array due to charge buildup will vary from -15 to +15 kv. During an orbit raising period, with the array biased to the plasma by the ion engines, voltages should be much less than maximum. Therefore, under worst case conditions the coverslides must stand off a maximum of 15 kv. Referring to Figure 6, a coverslide of 0.008 cm (3 mils) thickness would be sufficient. However, a safety factor of two has been assumed and a thickness of 0.015 cm (6 mils) is selected.

Two considerations could impact on this choice. Beginning-of-life open circuit voltage is employed in sizing. If the projected mission of orbit

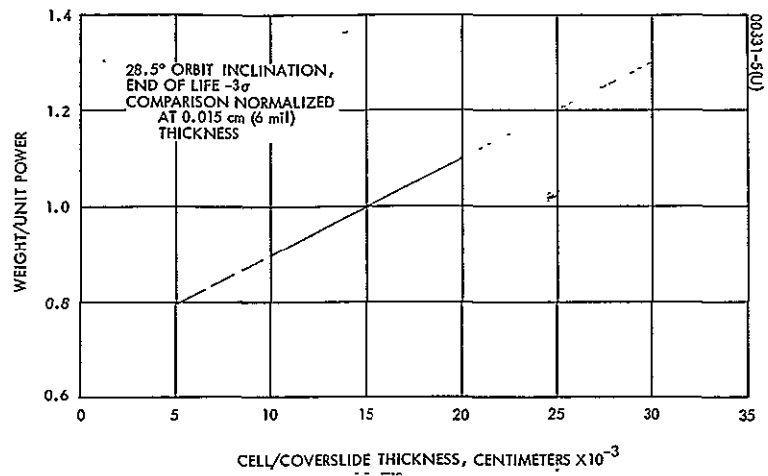


Figure 5. Weight-Efficiency Trend as a Function of Cell and Coverslide Thickness

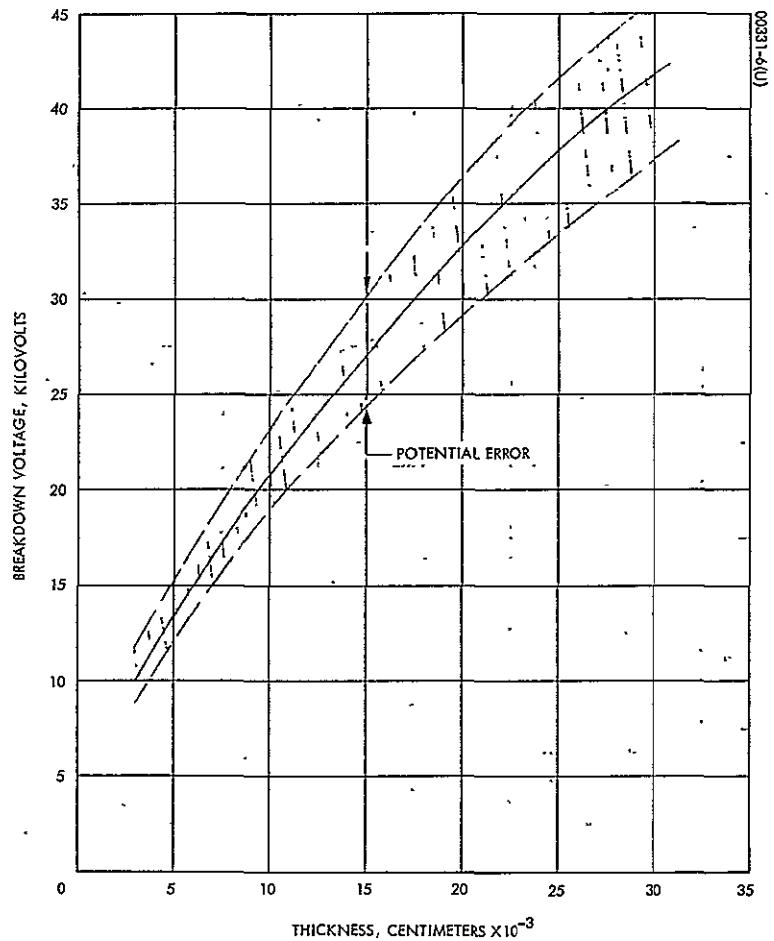


Figure 6. Dielectric Breakdown Voltage as a Function of Thickness for Fused Silica at 100°C

raising were chosen and communication was not begun until after orbit raising, the maximum open circuit voltage would have decreased due to radiation degradation.

Also, further testing is required to verify the assumed dielectric strength of quartz. However, 0.015 cm (6 mils) coverslides are considered a safe thickness for the array.

The final factor impacting cell/coverslide thickness is fabrication feasibility. This item is secondary in nature to this study. However, in the light of the large number of cells involved for the array and present fabrication technology, a total cell/coverslide thickness of 0.03 cm (12 mils) begins to approach a lower limit. The lower limit is established by acceptable attrition rates during fabrication.

Conclusions.

- 1) Cell type - 10 ohm-cm, boron doped, N/P silicon cell
- 2) A primary concern is cell and coverslide thicknesses
 - a) The cell and coverslide should be of equal thickness to provide equivalent front and backside radiation protection
 - b) The coverslide thickness required to stand off plasma charge buildup is 0.015 cm (6 mils)
 - c) The chosen thicknesses are 0.015 cm (6 mils) cells and 0.015 cm (6 mils) coverslides
- 3) The selected cell/coverslide thicknesses are within the limits of fabrication feasibility.

Buses and Interconnects

All buses are spaced at 50 volts per 0.0025 cm (1 mil) of separation. This spacing was chosen to allow enhanced dielectric protection and in-air test of the high voltage array. Such a criterion results in a very small weight and area penalty. However, the advantages for methods of testing and relaxed tolerances in fabrication are obvious.

In addition, it is recommended that all buses be unencapsulated. The simplistic approach of unencapsulated buses and spacing for in-air conditions counteracts the danger inherent in voids in the encapsulant and the encapsulant's degradation in the space environment. The pros and cons of encapsulation were entered in great detail in the already completed High Voltage Array Study (Reference 1). It may be shown in future breadboard tests that conformal coatings are required on certain isolated areas of the panel. Such a constraint would be introduced to protect critical regions of the panel from surface contamination and physical damage during fabrication and testing. However, full encapsulation cannot be recommended at

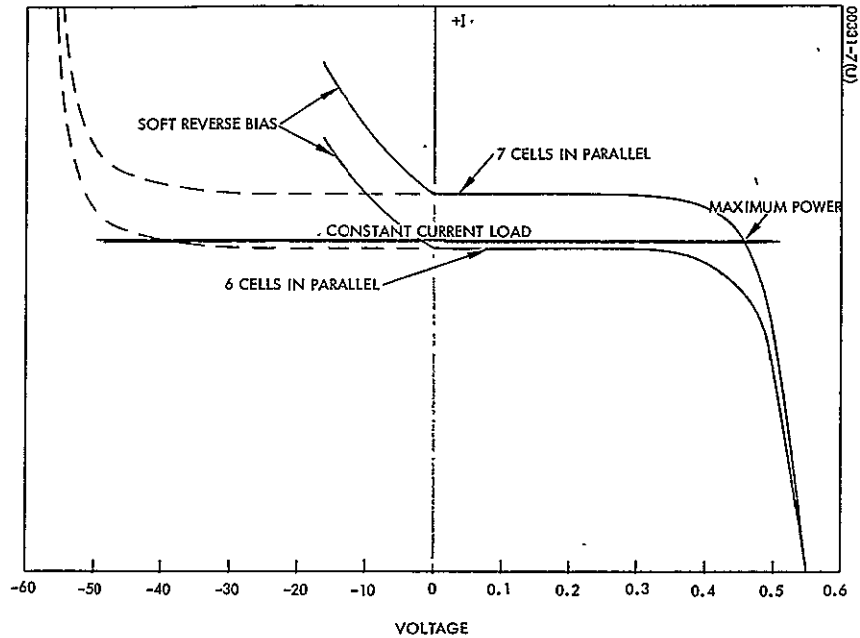


Figure 7. Effect of Open Circuit Cell Failure - Back-Biasing of Remaining Cells in Parallel

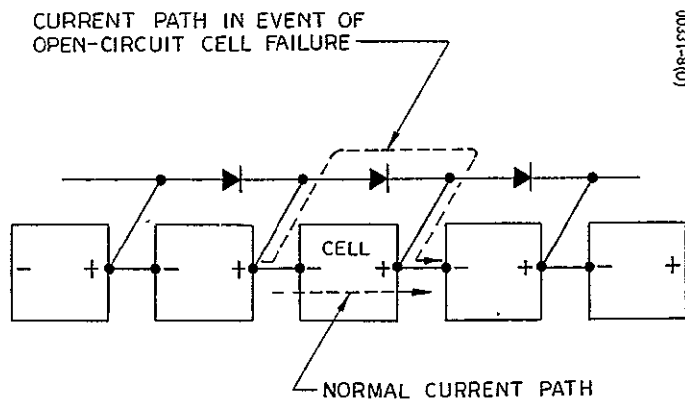


Figure 8. Incorporation of Bypass Diodes

this time unless the depressed current collection concept is used (Figure 23). Conductive surfaces should be exposed to the plasma environment to allow controlled current leakage and to inhibit the formation of destructive vapor arcs.

All buses should be placed on the front side of the panel. In conventional flexible arrays, it is common to configure buses on the array backside to conserve area. However, the danger of catastrophic through failures between buses and cell groups constrains bus placement to the front side only. Since the current levels for the high voltage array are so much lower than conventional arrays, the buses are sized to 0.25 cm width for comparable power loss. Therefore, the penalty for this design action is small.

No specific problems unique to high voltage arrays in the area of cell-to-cell interconnects are expected. In fact, the exposed and unencapsulated cell interconnects will serve an important function on the high voltage array; they will act as leakage current collectors to the plasma and thereby minimize the danger of vapor arc formation.

Conclusions. Buses are spaced for in-air test, unencapsulated, and placed on the panel front side. No unique high voltage interconnect problems are anticipated.

Array Failure Protection

A number of devices and actions are possible for failure protection on the high voltage array. These are common in principle to both array models.

Bypass Diodes. The probability of an open solar cell occurring in a single series string of cells is much higher on the high voltage array than on a conventional array. Such a condition exists because the high voltage array requires a larger number of cells in each series string. The primary concern in open cells is the potential for back-biasing the remaining cells in parallel with the open. The effect of opens and the resultant back-biasing is shown in Figure 7. With seven cells in parallel and a constant current load, the failure of a single cell would cause back-biasing, since the load could not adjust downward. As a result, in the back-bias condition, the power loss of operation at -40 volts would accrue. A secondary phenomena is the heating effect due to power dissipation and the resultant potential for a hot spot failure mode of operation. The method of protection from open failures chosen for this design is the utilization of bypass diodes. Figure 8 depicts the electrical function of the diode in bypassing the open failure.

The optimum number of diodes for a given array design depends upon three factors:

- 1) Open cell failure rate
- 2) Ratio of series cells to parallel cells

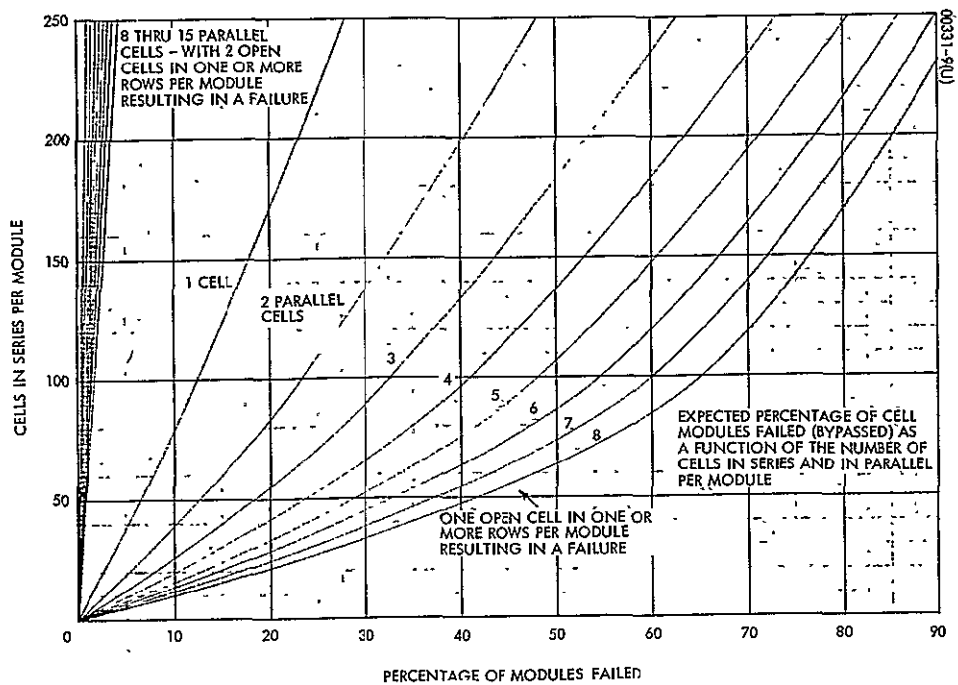


Figure 9. Expected Percentage of Cell Modules Failed (Bypassed) as a Function of the Number of Cells in Series and in Parallel per Module

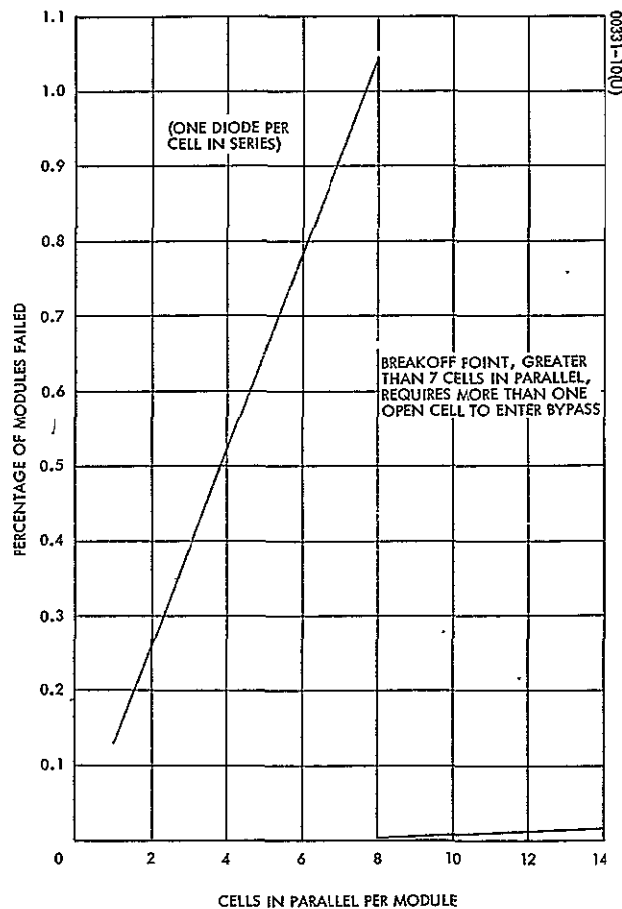


Figure 10. Module Failure (Bypass) Rate as a Function of Number of Cells in Parallel

- 3) Defined acceptable degradation in total array performance for the given mission

The cell failure rate employed is 3.0×10^{-8} /hr., or 0.001314 for the 5-year mission. This is pessimistic by a factor of four when compared to nonflexible arrays.

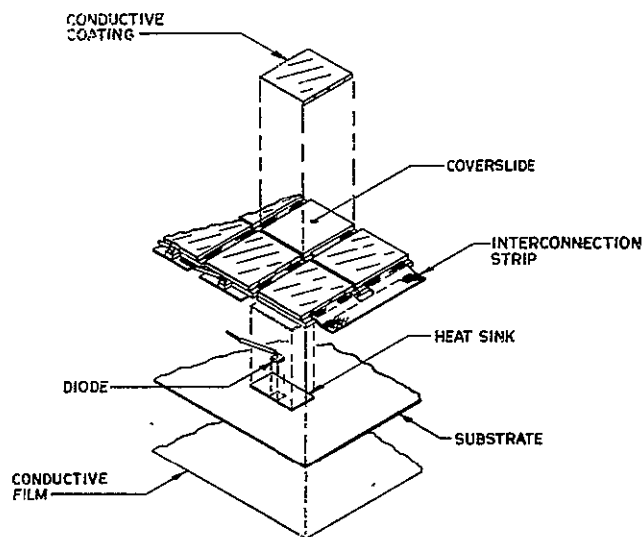
For a transverse cell layout, the cell parallel direction transverse to the drum axis, mechanical failure of the cells in the parallel direction can be considered random. Employing cell failure rate and random distribution of failure, software was developed in the previous High Voltage Array Study to predict the percentage of cell modules failed as a function of the ratio of series to parallel cells in the module. A module is a series/parallel group of cells with a bypass diode in parallel. Failure is entrance into a back-bias mode of operation, bringing the diode into operation. The results are shown in Figure 9. As can be seen, there is an increase in performance degradation with an increase in either the number of cells in series or the number of cells in parallel in the module up to eight cells in parallel. At that point there is a break in the trend. At eight cells and above in parallel, two cells, rather than one, in the same parallel row must fail to back-bias the remaining cells.

With greater than seven cells in parallel, it is possible to have a large number of series cells in the bypass module and maintain a low failure percentage. However, for fewer cells in parallel, it may become necessary to have a diode in parallel with each parallel row. The failure rate for the 5-year mission with one bypass diode per parallel row is shown in Figure 10. The same breakoff point at seven cells in parallel is shown for this special case.

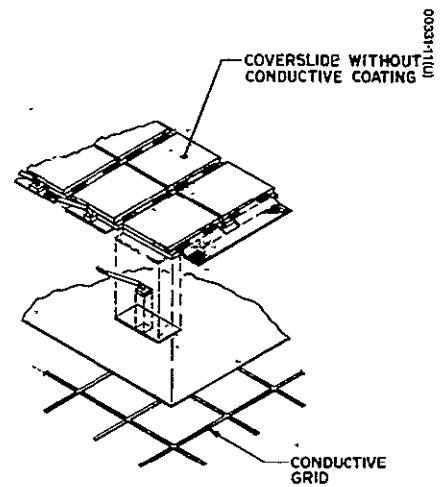
A typical diode for this operation is a Hughes developed diode chip which measures approximately 0.1 by 0.1 cm. The forward voltage drop is 1.1 volt at 1 ampere and 1.5 volt at 2 amperes. The diode has shown no property degradation at a radiation dose of 10^6 rads.

An alternate approach to bypass diodes was considered. Although this approach was not adopted, it should be given further consideration in the future. Figure 7 shows the back-bias characteristics of the solar cell. Most cells have a comparatively sharp back-bias characteristic. However, cells have been seen that have a soft-reverse bias. If such cells were available on a quantity basis, bypass diodes could be eliminated. It is not known at this time whether or not such cells could be reliably produced. For a large cell order, manufacturers might be willing to explore this characteristic.

Blocking Devices. The risk of failures due to short circuits on the high voltage array is minimized through the use of a dielectric substrate, the avoidance of wiring crossovers on the panel, front side placement of buses, and spacing of 50 volt/0.0025 cm (1 mil). However, the possibility of such failures remain and they can be catastrophic. Isolation devices can



FULL CONDUCTIVE COATINGS



CONDUCTIVE GRID ONLY

Figure 11. Methods of High Voltage Protection

be employed between all blocks and the main bus. Such devices should fulfill two requirements. First, the isolation must occur quickly/ and second, the isolation must be highly reliable, lasting for up to the full 5-year mission life.

Blocking devices will be discussed in more detail in Section 5.

Backside Conductive Grid. The only design item, excluding electronics, proposed for the high voltage array which is not common to conventional arrays is a backside conductive grid (Reference 1).

The grid is composed of conductive material and is placed on the back side of the substrate. It serves as an inhibitor to the formation of destructive vapor arcs. It is expected that the metallic interconnects on the panel front side will prevent vapor arc formation. However, the back side of the array is a continuous dielectric. The grid would provide sites for back side plasma leakage current collection, and also control the size of any through failures. The grid would be continuous on the block level and correspond to the front side block size. It would be connected through the substrate on a block level electrically. Such a grid is illustrated in Figure 11.

It should be emphasized that the necessity of such a grid requires substantiation by actual tests. If required, as expected, the optimum spacing and width of the grids will also be determined by test. Two factors must be considered: plasma protection and array temperature effects. As the area coated by the grid increases, array operating temperature at low altitudes will also increase.

Outgassing. Materials used in array fabrication are subject to outgassing in space. The primary source of outgassing is the RTV silicone adhesive being proposed. Typical outgassing rates for an RTV methyl-phenyl silicone and Kapton are presented in Figure 12. To prevent array failure due to Paschen type discharge, time should be allowed for outgassing to drop below the critical region prior to initial array turn-on. The critical region is defined as the outgassing rate which concentrates sufficient molecules of gas at the array surface for the mean free path of the molecules to be less than the conductor spacing. Paschen type discharge should be precluded if time is allowed for the mean free path of the molecules to become greater than the conductor spacing. Such techniques as bakeout during the manufacturing sequence could significantly reduce the required time for in-space bakeout.

Clamping and Isolation. The desirability of clamping and isolation for failure protection will be discussed in detail in Section 5. However, some of the reasons for considering the utilization of these techniques are listed below.

From the standpoint of outgassing, it would be desirable to clamp during the critical period mentioned above. Such clamping would be

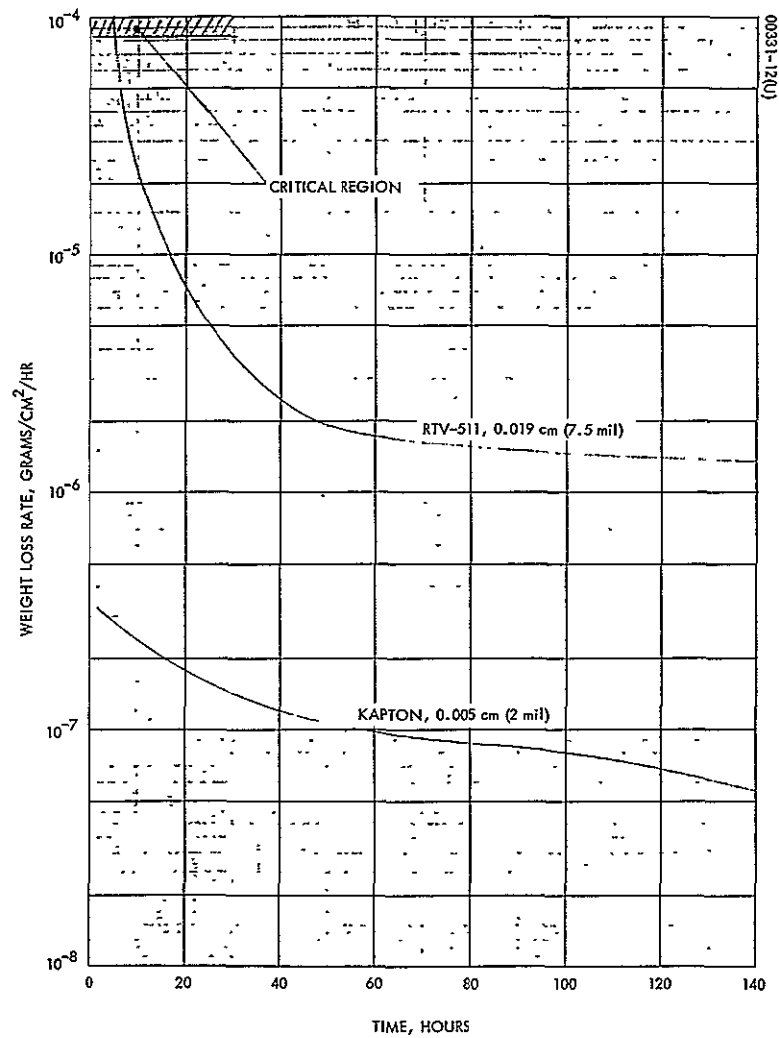


Figure 12. Typical Outgassing Rates (95°C, 1×10^{-5} Torr)

required only at the beginning of life, until outgassing rates drop below the critical level.

The other condition suggesting clamping is the transient high voltage at exit from eclipse, prior to array warmup. This is an extremely short term effect, for the array warms up quickly. However, the condition exists for the entire mission life. A possible alternative action is controlled array orientation, with the array front side pointed away from the sun at eclipse exit.

Isolation is desirable for both of the above conditions. Such isolation would prevent current flow between unbalanced blocks during clamping. These currents could damage electronic components.

Conclusions. Various failure protection devices and actions, as listed below, are possible and practical for high voltage arrays.

- 1) Bypass diodes will provide protection against open cell failures.
 - a) For greater than seven cells in parallel, one bypass diode for 50 cells in series will assure a failure of less than 1 percent of the modules for the 5-year mission.
 - b) For seven cells or less in parallel, one bypass diode for each parallel row is required.
- 2) An alternate approach to bypass diodes for open circuit protection would be the development and use of cells with soft reverse characteristics.
- 3) Blocking devices with fast response and high reliability should be employed for protection from shorting.
- 4) Excluding the electronics, the only unique design item for the high voltage array is the back side conductive grid. It may be necessary to inhibit the formation of vapor arcs and the spread of through failures on the panel back side.
- 5) The array should be allowed to outgas, following injection and extension, until the outgassing rates have dropped below the critical region in which Paschen type breakdown can occur.
- 6) Clamping and isolation are suggested procedures both during the initial outgassing period and at exit from eclipse.

Materials Summary

The materials chosen for the high voltage array were discussed in detail in the first High Voltage Solar Array Study. They are repeated here with a minimum of comments for the sake of completeness. An isometric view of materials is shown in Figure 11.

Coverslide: 0.015 cm (6 mil) fused silica

Cell: 0.015 cm (6 mil), 10 ohm-cm, N/P, boron doped silicon cell

Interconnects and buses: Copper

Diode: Typical diode chip, 0.1 by 0.1 cm

Diode Heat Sink: Copper strip

Back side conductive grid: Suggested - vacuum-deposited aluminum (VDA)

Full conductive coatings: These will be discussed in some detail in subsection 3.2.5. They may range from metallic to semiconductive.

Adhesives:

- 1) Cell to coverslide - R-63-489, Di-methyl silicone.
- 2) Cell to substrate - RTV 655, clear methyl-phenyl silicone. A clear cell/substrate adhesive is chosen to allow back side inspection during fabrication and to maintain lower maximum temperatures at low altitudes where the earth's albedo is a factor.

Encapsulants: Encapsulants have not been suggested for the array surface. They have been avoided because of the inherent danger of voids and dielectric degradation during a 5-year mission. If they should be proven desirable in future studies, RTV 655 would be preferred. Parylene is not recommended because of fabrication problems. The epoxies are discarded because of the degradation and adverse shift in their electrical properties in the environment.

Substrate: 0.013 cm (5 mil) Kapton. Kapton is the selected material because of its high dielectric strength and its stability under environmental stress. The chosen thickness is based on the need to stand off the charge buildup in a plasma environment. The maximum voltage standoff requirement is the same as that of the coverslide. This has already been discussed in detail. Based on beginning-of-life open circuit voltage for an array floating with respect to the plasma the substrate must stand off 15 kv. Such a voltage requires a 0.008 cm (3 mil) thick Kapton substrate. Following the factor of two safety factor already established in sizing the coverslide, a thickness of 0.015 cm (6 mils) of Kapton would be suggested. However, the thickest films of Kapton now produced are 0.013 cm (5 mils). The manufacturer indicates that he has no intention of increasing this thickness. Therefore, 0.013 cm (5 mils) is chosen for this design and is considered sufficient, pending future tests.

Conclusion. The pacing material items that cause adverse performance increments in respect to low voltage arrays are the cover-slide and substrate thicknesses. The validity of the sizing principles for these dielectric materials must be tested in follow-on work.

3.2.2 Problems in Fabrication and Testing

In general, both array models present the same problems. As the total array area increases, concern for fabrication and testing must also increase to reduce production costs. It becomes imperative to constrain the optimum design, in respect to performance, with fabrication and testing considerations.

Problems Common to High Power Arrays

Much effort has been expended in the conceptual design of large area arrays for operation at low voltages. However, the techniques to develop actual hardware have received limited attention. Few companies have been required to develop their arrays beyond a conceptual or model state. Without exception, companies conceptually design a multikilowatt array, and then actually build a several hundred watt array to establish feasibility.

Therefore, summary mention is made of problems common to large area arrays whether they are high voltage or low voltage. In general, this study assumes that the techniques for manufacturing and testing large area, low voltage arrays exist.

Size Limitations. The very size of the final panels creates problems for full array thermal-vacuum testing. Existing test facilities are limited in size. Undoubtedly, tradeoffs will be necessary to determine subsystem module sizes requiring full quantitative electrical performance tests under environmental conditions. Full system tests in a simulated space environment are desirable. However, certain functions can be tested under partial or pulsed illumination in ambient conditions. Recent developments in pulsed illumination for solar panel testing allow the testing of large panel areas with excellent illumination uniformity. For large areas, such systems can be developed for only a small portion of the costs of steady state systems. Size is also a factor in the handling and testing of the panel in a 1 g environment. The array is not designed for 1 g operation. Numerous techniques of array support for fabrication and deployment have been developed. They should be applicable to the large area array. However, the very size may place limitations on existing techniques. Certainly, existing facilities will require modification.

Mass Fabrication and Test Techniques. For the most part, manufacturing techniques for the mass production of solar panels have not been developed in the industry. Satellite systems have required a limited amount of solar cell power. As a result, funding has been associated with design and high quality panel fabrication. As array area increases, more of the costs will be associated with fabrication and test. Present efforts in the

TABLE 3. FABRICATION PROBLEMS AND CONSIDERATIONS

Evaluation	Types and Areas of Problems												
	Voids						Separations	Cracks and Tears	Wrinkles	Contamination		Process Control	
	Coverslide	Coverslide Adhesive	Cell Adhesive With Scrim	Cell Adhesive Without Scrim	Laminated Substrate	Substrate Film	Adhesive	Substrate	Substrate, Substrate Adhesive	Environmental	Fabrication	Conductive Coatings	Electrical Interconnections
Effects	Possible electrical discharge site, dielectric erosion	Site for initiation of dielectric failure	Site for initiation of dielectric failure	Site for initiation of dielectric failure	Site for initiation of dielectric failure	Site for initiation of dielectric failure	Similar to voids	In high stress area acts as void, mechanical	Cracks upon flexure	Electrical shorts, leakage currents, outgassing	Electrical shorts, leakage currents, outgassing	Shorts, electrical stresses	Opens, intermittent
Probable occurrence scale 10 to 7 severe, always, 6 to 3, moderate, limited, 2 to 0, light, slight	0 to 1	0 to 2	8 to 10	1 to 8	0 to 2		All adhesive areas 1 to 4	1 to 2	5 to 10	1 to 2	5 to 10	0 to 1	
Allowable level	Not allowed at erosion level	Established by electrical stress in given area, volts/cm	Established by electrical stress in given area, volts/cm	Established by electrical stress in given area, volts/cm	Established by electrical stress in given area, volts/cm	Established by electrical stress in given area, volts/cm	Established by electrical stress in given area, volts/cm	Small surface cracks allowed - otherwise treated as voids	Wrinkles not producing cracks			Established by electrical stress in given area volts/cm	Opens or intermittents not allowed
Method of detection	Visual	Visual	Electrical, omission discharge methods	Electrical, omission discharge methods			Visual, electrical stress, ultrasonic	Visual	Visual, radius gauge	Surface resistance, electrical	Visual, electrical, fluorescent, surface resistance	Electrical stress	Electrical, visual (under flexed conditions)
Method of elimination	Rejection of coverslide	Rejection, process control	Reduced by viscosity control, conductive adhesive	Reduced by viscosity control and degassing	Resin control, roll lamination		Process control, viscosity	Controlled bend radii, processes, repair	Flat working surfaces, handling control	Cleaning procedures, handling, storage	Post operative cleaning methods, inspection	Process controls, repair techniques	Process controls, rework

industry to develop modular cell group production through mass joining techniques require greater emphasis. Duplication of processes with identical segments of the panel for both fabrication and testing will result in cost savings. Panel production will become a full-fledged repetitive manufacturing process. Designs that lend themselves to such techniques will become a necessity. The conceptual designer will be required to know the manufacturing processes at a depth unnecessary in the past.

Problems Unique to the High Voltage Array

Dielectric Considerations. An awareness of potential problem areas in the fabrication of dielectric configurations is essential in the manufacturing of the array. This heightened concern is necessary for both the panel fabrication and control electronics packaging. A summary of problem areas in the fabrication process is shown in Table 3. The particular areas of concern were entered in detail in the completed High Voltage Solar Array Study.

The dielectric configurations in the two proposed array models have been sized to allow in-air test of panel electrical performance. Such design consideration costs little in terms of weight and allows relaxed tolerances in fabrication.

Safety. Special consideration must be given to personnel safety in the fabrication and testing of high voltage arrays. This constraint was reported in detail in the High Voltage Solar Array Study. "Safe" current levels have been established. The fabrication sequence will be defined to allow full panel fabrication prior to final interconnection of panel sectors and entrance into a potentially hazardous condition. In addition, pulsed illumination of large panel areas for electrical tests will limit the severe hazard to personnel.

Control Electronics and Panel Integration. The required placement of control electronics on the high voltage panel results in design constraints. The optimal panel design must allow the functional test of the control electronics together with the associated solar cell power block. Two conceivable approaches are possible.

First, all regulation and reconfiguration electronics may be located in a small area at the base of the panel. Such a configuration is proposed for the specific array model. As a result, the control electronics may be tested in its entirety with a power source simulating the panel. The panel itself may be fully fabricated and quantitatively tested for electrical performance on a sector basis. A qualitative test of the final full panel with control electronics may then be performed.

The second approach, the universal array model, employs intermediate control logic adjacent to the controllable block. Placement of intermediate electronics outboard of the panel results in area constraints on the block size. The block should be small enough to allow a block system test with associated intermediate logic. Although steady state illumination would appear desirable for such testing, pulsed illumination may suffice.

Continuous illumination is desirable principally for investigations of closed-loop transient response, regulation accuracy, and loop stability. These factors of performance, however, are dependent on the design approach used and once these are verified by a model or continuous operation of a subpanel system with an actual load or load simulator, it should be possible to project satisfactory total system operation (and correct fabrication) by qualitative and quantitative information gained through pulsed illumination testing. Such testing would verify interconnections, switch operation, sector voltage magnitudes, and coupling between panel electronics and on-board-control electronics. The time duration of each pulse of pulsed illumination should allow the testing to be done by sequential stepping of the states of the regulation and control switches. By correlating measured data with the programmed system states satisfactory operation could be inferred.

The two approaches to control electronics have been presented to heighten an awareness of the impact of testing on the conceptual design of a high voltage array. Placement of control electronics on the panel presents unique and interesting problems to conceptual design. The optimum array from the standpoint of load matching efficiency may not be the final chosen array.

Conclusions

- 1) As array area increases, the impact of fabrication and testing techniques on the final array design also increases.
- 2) Pulsed illumination offers considerable advantage over steady state illumination for quantitative and qualitative tests of large area panels.
- 3) Considerable effort will be required in the industry to refine mass production techniques for solar cell groups.
- 4) Control of potential dielectric problems will necessitate heightened awareness of the cause of such problems by personnel during the fabrication process.
- 5) Dielectric configurations should be sized to allow in-air ambient tests.
- 6) Techniques for the control of hazardous high voltage conditions during fabrication have been proposed and must be rigidly enforced.
- 7) Placement of intermediate control electronics on the panel requires size limitations to the controllable block. Such limitations relate to test restrictions.

3.2.3 Configuration Methods

Configuration, in detail, will be handled in the layout of the two chosen models. However, three common items exist.

First, if a rollup deployment system should be chosen for the final array design, the parallel direction of cell layout should be in the direction transverse to the drum axis. This alignment decreases the potential for multiple open failures in a parallel row (see Figure 13).

Although the contract requires comparison of the high voltage array with a conventional rollup array, foldup configurations are feasible. In general, the design principles and concerns developed in this study are independent of the deployment system. As has been indicated, the two models will be configured as a four panel rollup array for comparison with the conventional array. Typical array configurations are shown in Figure 14.

Finally, although it may prove desirable to control voltage gradients by block arrangement, such control is related solely to conventional high voltage dielectric concerns. Voltage gradient control has little or no effect on plasma problems, and the technique is not utilized in the proposed models.

3.2.4 Array Performance Prediction

The total array performance is independent of the specific configurations of the two models. The final sizing of the array is based upon environmental effects for the proposed 5-year orbit raising mission. The array is sized to provide the required end-of-life power. Particular consideration is given to the predicted out of eclipse I-V characteristics of the array.

Environmental Effects

Temperature. Although the array temperatures are not unique to high voltage, they are presented for design reference. The temperature extremes have an impact on array performance and sizing and out of eclipse voltages. They also influence the specialized electronic device performance and the sizing of dielectrics. Dielectrics are sized for maximum temperatures. Maximum and minimum equilibrium illuminated temperatures are presented as a function of altitude in Figure 15. Temperatures are higher at lower altitudes as a result of the earth albedo influence.

The instantaneous out of eclipse temperatures are of particular concern in the design of the array. These temperatures create the condition for extremely high open circuit voltages as the cold array is initially illuminated prior to warmup (see Figure 16). As with the illuminated conditions, the temperatures are higher at low altitudes because of earth albedo effects. This condition exists briefly, in the order of 5 to 10 minutes, the time required to achieve equilibrium illuminated temperature.

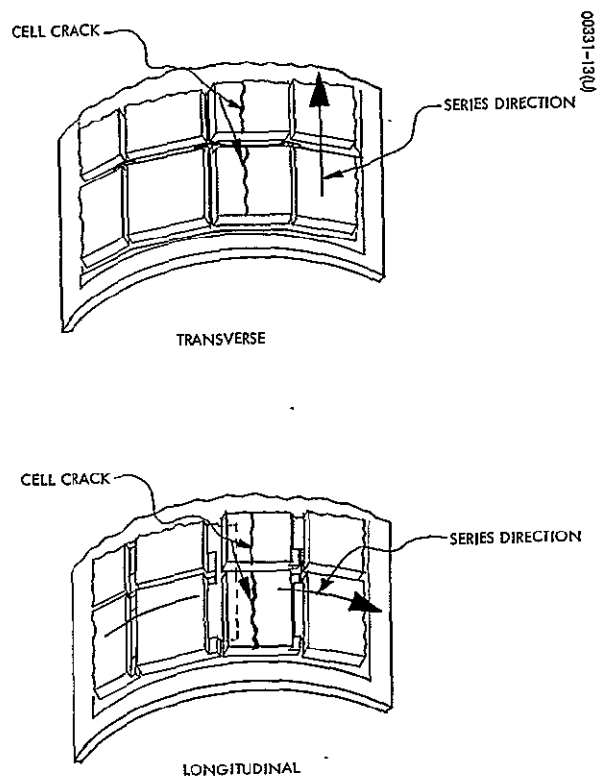


Figure 13. Expected Open Cell Failures as a Function of Series Orientation

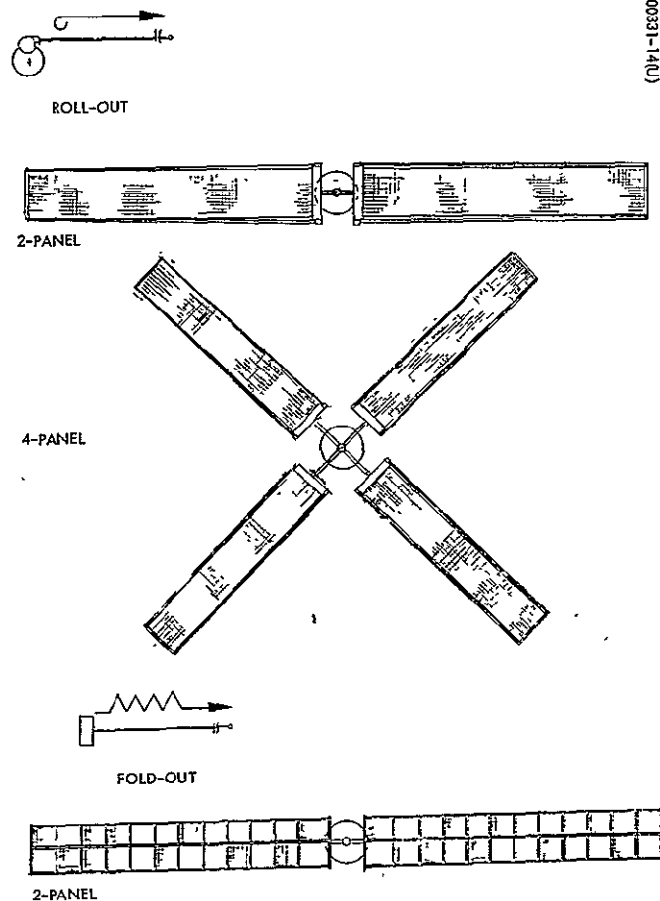


Figure 14. Typical Solar Array Configurations

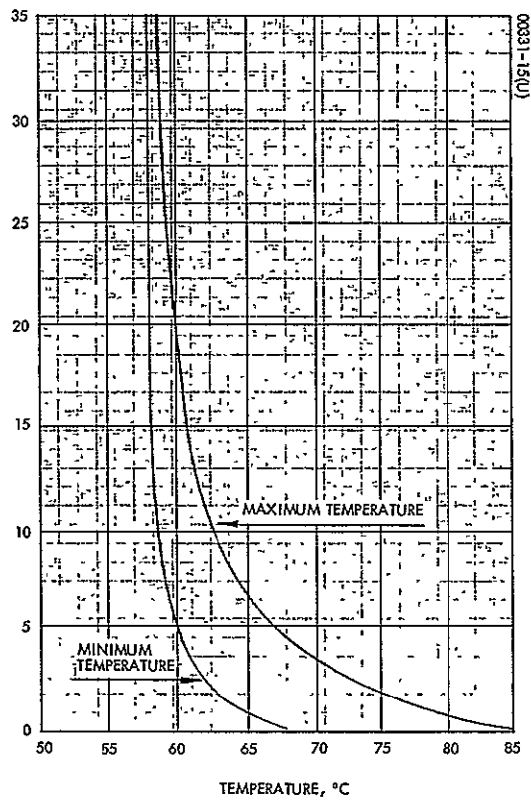


Figure 15. Maximum and Minimum Temperatures During Circular Orbit as a Function of Orbit Altitude

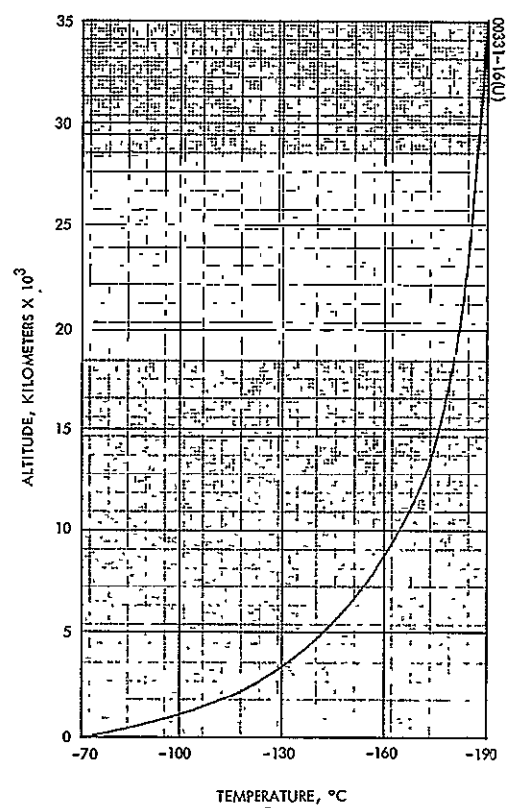


Figure 16. Minimum Eclipse Temperature for Maximum Duration Eclipse During Circular Orbit

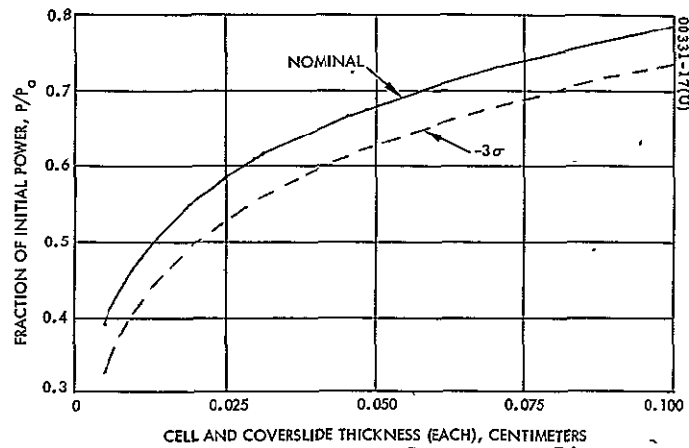


Figure 17. Radiation Degradation as a Function of Cell and Coverslide Thickness (28.5 Degree Orbit Inclination, End-of-Life)

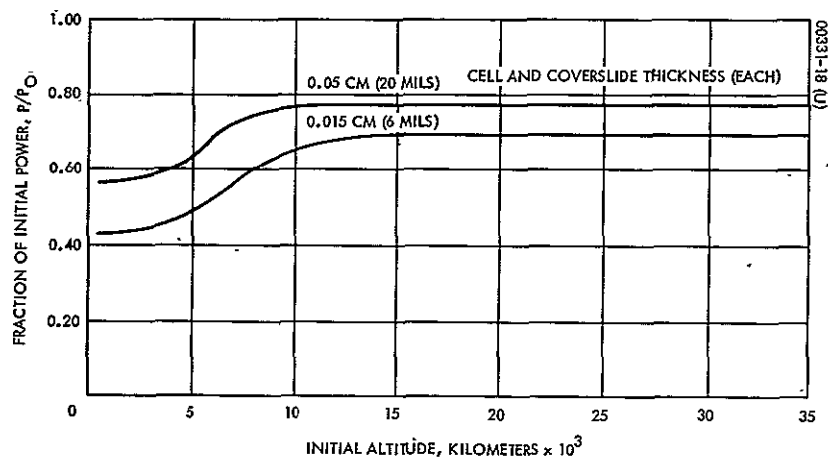


Figure 18. Radiation Degradation as a Function of Initial Injected Orbit Altitude (0 Degree Orbit Inclination, -3σ)

Particulate Radiation. Considerable effort was directed toward definition of the radiation environment for the orbit raising mission. Since the environmental effects are not limited to high voltage arrays, the results will be presented with a minimum of detail. The methods of calculation are presented in Appendix A.

As was noted in the discussion of optimum cell/coverslide thickness, back side radiation effects must be considered for cells mounted on thin flexible substrates. The optimum thickness is equivalent cell and coverslide thickness.

The chosen thickness was 6 mils to minimize weight/unit power and to withstand plasma charge buildup. The degradation in array power due to radiation effects is shown in Figure 17. It is presented for various equivalent cell/coverslide thickness combinations. The -3σ value reflects the factor of 2 uncertainty in the NASA maps. A 28.5 degree orbit inclination is assumed which results in approximately 10 percent less degradation than a 0 degree launch.

It might be mentioned that degradation occurs primarily in the Van Allen belts during the orbit raising phase of the mission, 91 days, rather than during the time at synchronous orbit. End-of-life radiation degradation as a function of injection altitude is shown in Figure 18. Solar flare activity for a 5-year orbit raising mission with an assumed launch date of 1972 is at a minimum (see Appendix A). Contribution to degradation for low altitude injection is negligible. Solar flare effects have been included at synchronous orbit but amount to only about 2 percent for the selected launch date. Degradation due to solar flares will be a function of predicted flare activity for the mission period. Therefore, a change in assumed launch time could have a significant effect on predicted degradation for injection above the Van Allen belts. Note that 0 degree orbit inclination is assumed in Figure 18 and that only -3σ values are given. The approximate difference between nominal and -3σ values is apparent in Figure 17.

There is no desire to overemphasize radiation effects which also impact on low voltage arrays. However, the predicted degradation becomes a factor in array sizing. As a result of the required additional cells to meet end-of-life power requirements, beginning-of-life open circuit voltages under illumination and at exit eclipse can be very high. The delta power over the mission life also impacts on the range and flexibility of control electronics requirements.

Electrical Performance

Prediction of total array performance employs Hughes software. The software statistically takes into account the numerous factors influencing current and voltage. The factors incorporated in the software are temperature, intensity, radiation, fabrication loss, coverslide transmission loss, and instrumentation allowance. Beginning and end-of-life I-V characteristics of the array are shown in Figure 19. Knee softening effects due to temperature and radiation have been included in the curve shapes.

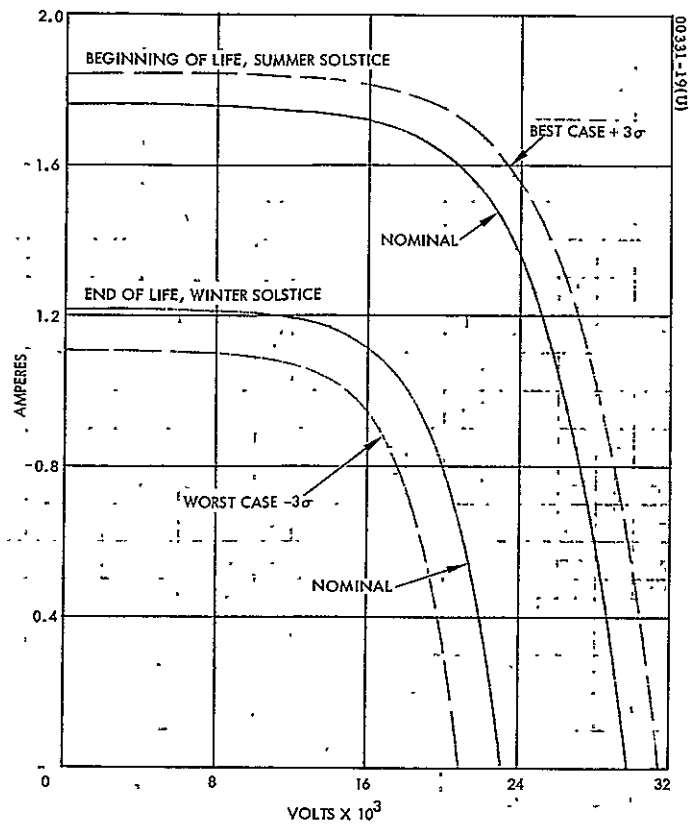


Figure 19. High Voltage Solar Array Performance Optimization for 16 kv

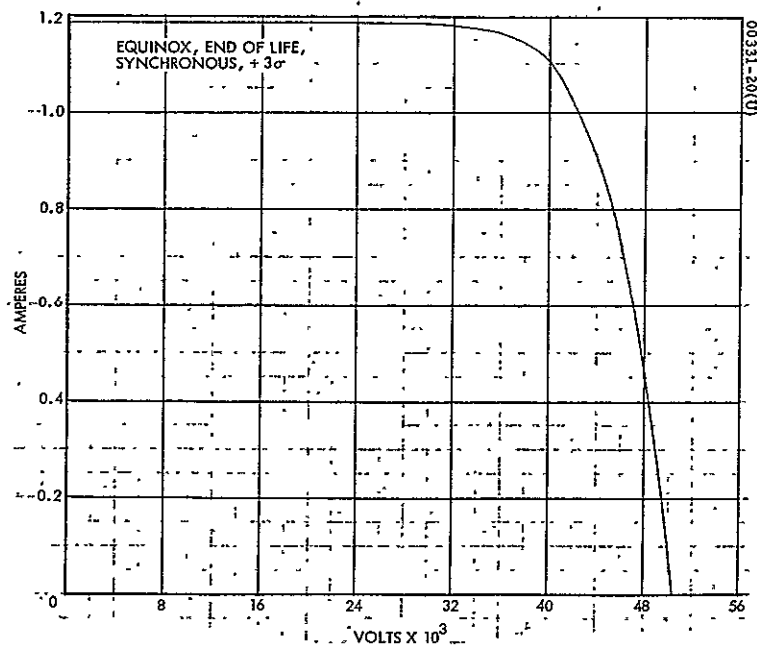


Figure 20. High Voltage Solar Array Post-Eclipse Performance

Based on mission life and degradation factors, approximately 71,000 solar cells in series are required to meet the end-of-life, 16 kv requirement. In addition, 14 cells in parallel are necessary for 0.94 ampere to fulfill the 15 kw requirement at the end of the mission.

Out of Eclipse Performance

The temporary high voltage as the array exits eclipse is of basic concern to the array design. The post eclipse I-V characteristics are shown in Figure 20. The $+3\sigma$, end-of-life condition is chosen as worst case. End-of-life conditions may be employed for the proposed mission since all but a negligible portion of radiation degradation has occurred during orbit raising and prior to reaching synchronous orbit. Maximum voltage is employed at synchronous orbit for communication. The worst case maximum open circuit voltage at eclipse exit is 50 kv, or voltage gradients of ± 25 kv for a floating array.

It should be repeated that dielectrics on the array were sized for maximum illuminated open circuit voltage at beginning of life. Protection from the potentially high voltages at eclipse exit will require isolation and possible clamping of blocks during the few minutes of warmup. These methods will be discussed later in Section 5.

Conclusions

- 1) The primary temperature effect in array design is the low eclipse exit temperature at synchronous orbit. It impacts on control electronic packaging mounted on the panel and produces high temporary voltages at exit from eclipse.
- 2) The particulate radiation damage effect on performance for an orbit raising mission is severe. However, judgement on the feasibility of the mission awaits total mission analysis and trade-offs. In spite of the degradation, performance is favorable when compared to low voltage arrays. The radiation studies highlight certain items to be considered in mission analysis:
 - a) Orbit Inclination. Degradation was seen to be decreased by approximately 10 percent by a 28.5 degree launch as compared to 0 degree
 - b) Injection Altitude. The degradation occurs, primarily, during the orbit raising phase of the mission
 - c) Backslide Radiation Effects. Further work may be required in assessing the design principles proposed in the estimates of these effects
 - d) Annealing of Radiation Damage. The potential of future improvement of annealing techniques should be considered

- 3) Although radiation degradation is common to both high and low voltage arrays, it does have potential secondary effects on high voltage arrays, particularly in increasing the ΔP over which the control electronics must operate.
- 4) To fulfill the array requirements of 16 kv and 15 kw at end of life, approximately 71,000 cells in series and 14 cells in parallel are required.
- 5) Worst case maximum open circuit voltage at eclipse exit is ± 25 kv for a floating array. Array protection from this voltage will be accomplished through isolation and, possibly, clamping.

3.2.5 Alternate Actions

Certain alternate design actions, mission changes, and load requirements are possible which impact upon the design and configuration of both array models in a similar fashion.

Conductive Coatings

It has been indicated that the primary penalty in high voltage array design, when compared to conventional low voltage arrays, is the required thickness of substrate and coverslide to withstand plasma charge buildup. One approach to breaking this thickness barrier is to employ conductive or semiconductive coatings on the coverslides and over the entire back side of the array. Such coatings would effectively bleed off the charge buildup and reduce the required dielectric thickness. These coatings were discussed in considerable detail in the first High Voltage Solar Array Study and will not be entered in depth in this study. However, their potential importance is shown in the performance increments presented at the conclusion of this study.

Such coatings would be limited to the coverslides on the array front side. Each coverslide coating makes electrical contact with the cell interconnect (Figure 11). The coating can be continuous on a block level on the back side. To limit voltage stresses through the dielectric, the coating would be biased to the front side on a block level. The electrical function of the coatings is shown in Figure 21.

Certain limitations, as listed below, exist in the proposal of conductive coatings.

- 1) Transmission - Although optical transmission is not a problem for the back side and a metallic film may be employed, the front side must have films with high transmission and limited environmental degradation. At present, such films with greater than 90 percent transmission have not been located. A complicating factor is that a minimum of 1 micron thickness is suggested to avoid coating loss at low altitudes due to sputtering. It is projected that developmental work in this area can produce a stable

coating with 95 percent transmission. Loss due to transmission imposes the penalty of additional cells. It is repeated that the coating may be conductive or semiconductive.

- 2) Current losses due to plasma leakage will be increased with conductive coatings.
- 3) It should be added that testing may indicate:
 - a) That conductive coatings are unnecessary because the self-imposed safety factor of two in dielectric sizing is not required.
 - b) That the added thickness of the substrate is necessary for structural support of the large array area.
- 4) Tradeoff between fabrication feasibility and weight savings may lead to the acceptance of the weight penalty for no conductive coatings.

In the performance increments, high voltage arrays will be considered both with and without conductive coatings. In these estimates, it will be assumed that a coating with 95 percent transmission can be developed.

Low Current Loads

The requirement for very low current loads could exist for a high voltage array. The two arrays being proposed for this study have limitations in this area. The simplified specific mission model has common current blocks of 0.94 amperes, end of life. The universal mission model has minimum current blocks of 0.068 ampere, end of life.

If such low current requirements are developed, a conceptual high voltage cell is proposed as one solution, (Figure 22). The cell is basically a conventional 2 x 2 cm wraparound contact N/P silicon cell. It has been sliced apart and rebuilt with a dielectric adhesive, forming a multijunction device. Such a device could provide 0.012 ampere at 4.5 volt, beginning of life.

Experimental work in multijunction cells is in progress in the industry. The final development of a high voltage cell would probably depend upon a demand for such a cell in other areas as well as the high voltage array. To produce such a cell, it must be proven profitable.

Redefined Mission

In the previous high voltage study (Reference 1) it was stated that the array could be operated above 3000 km at voltages up to 16 kv when floating and 6 kv when positively biased to the plasma with less than 5 percent power loss. A 2 kv biased operation in the ionosphere would cause 20 to 30 percent loss of power during the first few days of orbit raising, however, the

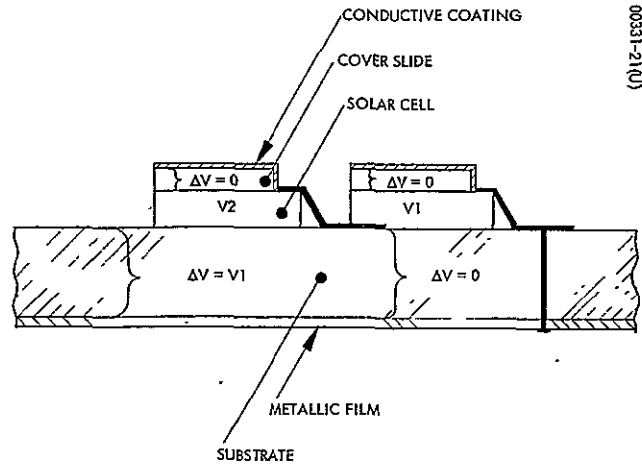


Figure 21. Electric Stress for Biased Dielectrics

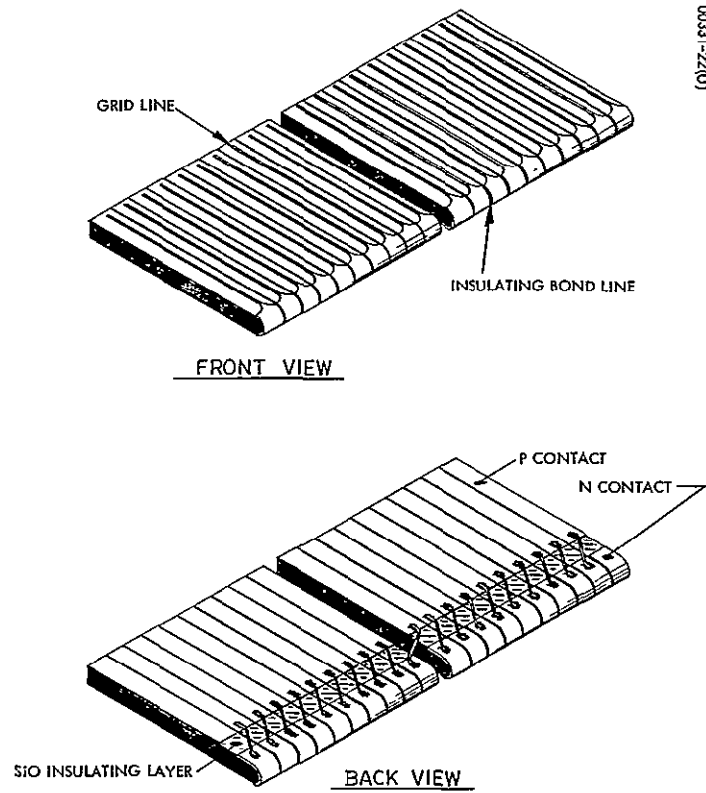


Figure 22. Conceptual High Voltage Solar Cell

radiation degradation has not occurred and such a temporary loss is tolerable. Such losses are for an array without special devices for reduction of leakage current losses, and would satisfy the mission requirements.

However, two factors could influence these statements:

- Unexpected processes contributing to degradation, as demonstrated in follow-on testing.
- Redefined mission requirements which necessitate operation at high (>2 kv) voltages in the ionosphere with the array biased to the plasma.

In the light of these factors, two devices were proposed in the previous study to reduce leakage current losses and to inhibit the formation of vapor arcs. They are briefly described here. It is emphasized that they are considered design alternatives, if, and only if, proven necessary in follow-on tests.

The method of depressed current collection is shown in Figure 23. The cell interconnects are encapsulated with a dielectric and a conducting plasma current collector is placed on the dielectric surface. The conductor serves two purposes:

- 1) To suppress pinhole arcs, serving as a current collecting electrode.
- 2) To reduce losses which would occur to the cell interconnects.

Losses are reduced by operating the collector at a voltage just high enough to collect all of the electrons entering the plasma sheath. The array power losses are determined by the collector voltage rather than the array voltage. Since a several hundred volt potential should suffice to collect all electrons, a power loss reduction by a factor of 10 may be possible.

The second device is a biased screen. Plasma leakage losses could be reduced by surrounding the array with a screen biased negatively to the space potential. Such a screen would reflect most plasma electrons. It is expected that losses could be reduced by an order of magnitude. Light intensity loss due to the spaced conductive wires would be approximately 1 percent. The screen, discussed in considerable detail in the completed High Voltage Array Study, is shown in Figure 24.

Degradation Compensation

The final alternate design action is compensation for particulate radiation damage. Although annealing methods through adjunct heating and back biasing of the array were considered, it appeared outside the scope of this study to enter them in detail. Radiation effects are common to both high and low voltage arrays. However, if the orbit raising mission is chosen, follow-on effort might be directed to this area. Further work is

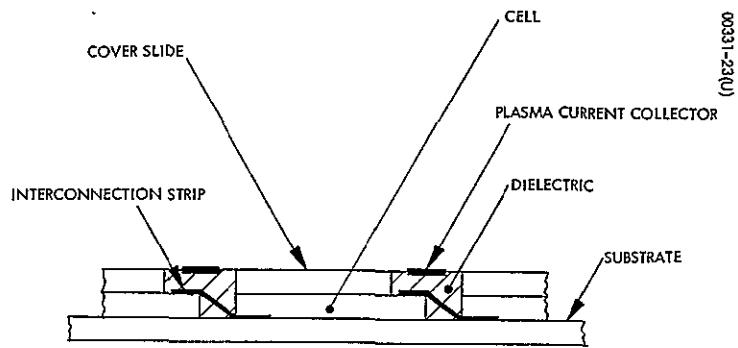


Figure 23. Depressed Current Collector Concept

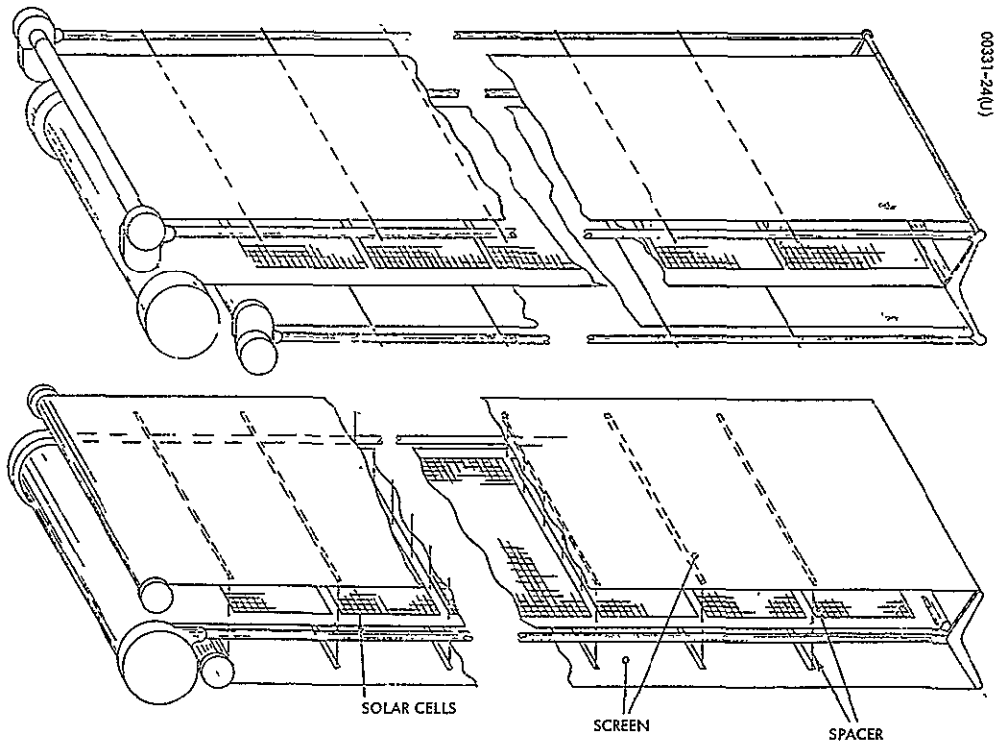


Figure 24. Plasma Screens

required to evaluate the potential of annealing and such concepts as partial and progressive deployment of the array.

Conclusions

Alternate design actions and requirements which would impact on the two proposed array models are listed below.

- 1) The substrate and coverslide thickness could be reduced through the use of conductive or semiconductive coatings. Such coatings would require developmental work. But they could eliminate the primary weight penalty imposed in high voltage operation of flexible arrays.
- 2) Mission requirements of very low current loads could be met through the development of a multijunction high voltage solar cell.
- 3) Although the proposed array models allow operation in the plasma environment for the proposed mission, other missions might require adjunct plasma protection. Such missions involve operation in the ionosphere at voltages >2 kv with the array biased to the plasma. Two devices which would reduce leakage current losses and inhibit vapor arc formation are the depressed current collector and the biased screen.
- 4) Emphasis on methods for compensation for radiation degradation to array performance are suggested for future work.

This concludes the discussion of elements common to both the universal and specific array models. The array models will now be configured in sufficient detail to allow the development of performance increments.

3.3 CONFIGURING THE ARRAY MODELS

Two array concepts have already been discussed, the universal and the specific. As the names suggest, the universal is independent of mission, while the specific is mission optimized. In the discussion of the two concepts, models of each were chosen to be developed as arrays for performance prediction. Preceding discussions were directed to design details common to both models. In this section, each array will be laid out in its uniqueness.

Bear in mind that two models are being developed in this study. The universal model represents a more pessimistic boundary for high voltage arrays. The specific is optimistic. The boundaries are developed for the performance estimates at the end of this report.

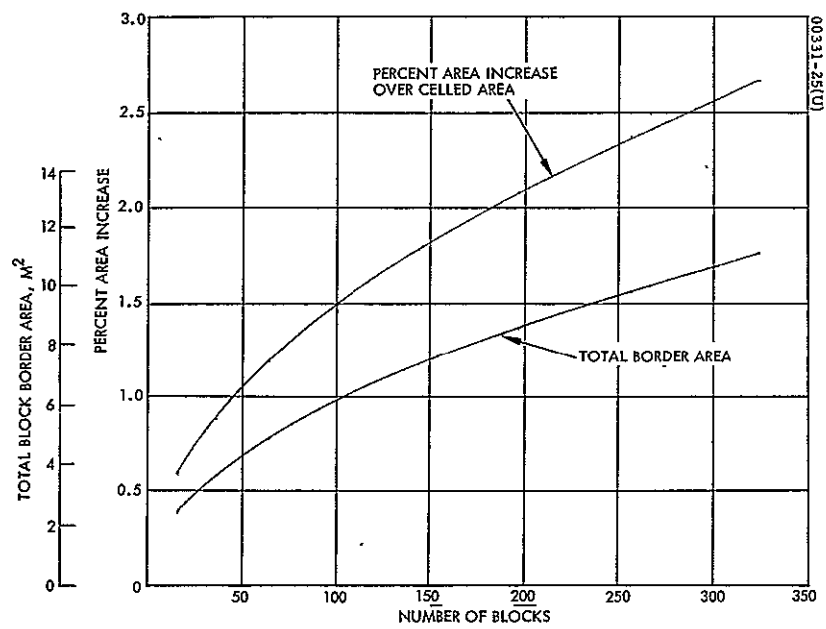


Figure 25. Substrate Area for Block Borders as a Function of Number of Blocks, Universal Approach

3.3.1 The Universal Model

One of the four identical panels of the universal array has been shown in Figure 3. There are 45 I-V blocks on the panel, allowing ± 250 volt voltage precision and ± 0.5 2 x 2 cm solar cell current precision.

The panel aspect ratio is kept the same as the base low voltage array given for performance estimates. The blocks have been maintained as square as possible for the most efficient use of area. This minimizes the border area and the impact of buses. Figure 25 presents the area lost due to borders, spaced for high voltage conditions. The figure assumes square blocks and neglects loss due to bus area. The losses due to buses can contribute appreciably to the area penalty, so care must be taken in using Figure 25 to make design decisions. The universal model configured in this study employs 180 blocks and requires a bus area in excess of two times the area loss to block borders.

The panel in Figure 3 has the 500 volt blocks located at the panel base for two reasons. First, regulation of the universal model employs only 500 volt blocks. Base location minimizes the length of regulation leads. Second, since the 500 volt blocks are smallest, they have the largest bus area for total area and buses should be kept shorter by base location.

The interconnection of blocks is accomplished through a combination of switching and hardwiring. The hardwiring patterns are changed from mission to mission. The location of the switching and hardwiring is shown at the base of the panel. It is an area 0.076 by 4.7 meters, the width of the panel. Area might be saved by placing this section between the 500 volt blocks and 1000 volt blocks. However, this would increase the length of the buses to the loads.

The buses extend from the bottom of each block to the panel edges. The cells are folded up and then down in each block, so that the negative and positive points of connection are both at the bottom of the block.

There are an odd number of blocks in most rows on the panel. In these cases, the buses from the center block are brought out to alternate sides of the panel to balance the edge area for buses.

The buses to the loads are shown at the bottom of the panel. There are 12 leads to the loads, each requiring 1.8 cm, which includes a 0.25 cm bus and the spacing for high voltage. Twelve leads are required, since any of the six simultaneous loads may require blocks of power from all four panels at once.

A detailed section of the universal model panel is presented in Figure 26. A portion of a 500 volt block with two cells in parallel is shown. It is located at the panel edge. The buses for each block are paired at the panel edge with 0.13 cm separation. Individual buses are 0.25 cm in width, and pairs of buses are separated by 1.5 cm for high voltage protection. Buses are unencapsulated. As was noted above, the cell groups

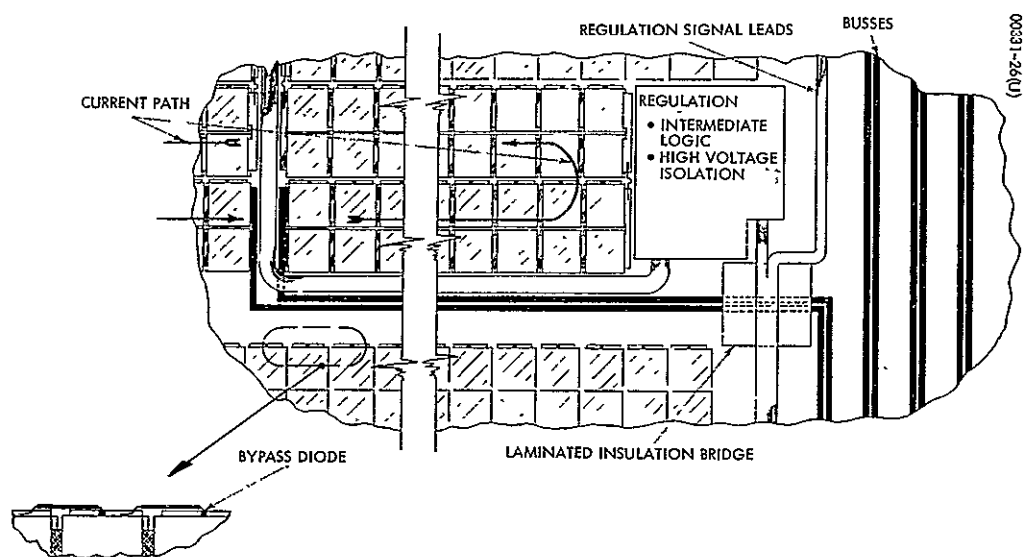


Figure 26. Solar Panel Detail, Universal Approach

are folded up and back within the block. This allows both negative and positive bus connection at the bottom of the block.

Since all cell groups have less than eight cells in parallel, all blocks have one, two, and three cells in parallel; one bypass diode is employed for each parallel row. The rationale for this decision was presented above under Failure Protection. One diode per row will maintain the row failure rate, due to bypass, below 1 percent for the 5-year mission.

The 0.1 cm diode chip is shown in Figure 26 mounted to a copper strip at the edge of the two-cell parallel row. The strip is approximately 0.25 cm in width, with one-half of it extending beyond the edge of the cell. The diode mounting strip provides adequate heat sinking. As will be seen in the performance increments, array area increase for bypass diodes on each cell row is 3 to 4 percent.

Intermediate logic for regulation is represented on the detailed drawing by a single block. For simplicity, it is not divided into its separate portions. However, the intermediate logic together with its function of high voltage isolation will be discussed in detail in Section 4. Regulation is applied only to the 500 volt blocks. There are six leads per 500 volt block, redundant sets of three. The leads run inside the buses with crossover extension. All the leads going to the individual block from the intermediate logic are at the same potential. Therefore, they are all in a single shielded cable; 0.025 cm diameter round wire should be sufficient for the individual regulation leads to the blocks. A dielectric bridge must be employed for the regulation leads for bus crossover prior to and after high voltage isolation. Such dielectric bridges, whether laminated or machined, should present no problems. Crossover of active leads has been eliminated in all other areas of the panel design.

In summary, Figure 3 represents the universal array model for the performance increments at the end of this study.

3.3.2 The Specific Model

In general, the specific array concept involves computer optimization of the array I-V blocks to the mission required loads. Initial software for this purpose has been developed and will be discussed in the summary of this section. One of the four identical panels of the model chosen to represent the specific concept is shown in Figure 4. As has been suggested, this is a simplified model. It assumes that the six simultaneous loads for the given mission can be met by sixteen 1 kv blocks with fourteen cells in parallel, 0.94 ampere, end of life. Figure 4 configures four of the sixteen blocks. Although such an assumption, a simplified panel to match a specific mission, is rather gross, it does allow configuration of an optimistic model for performance prediction. As a result, it is felt that the actual performance of a high voltage array will be bracketed by the two models.

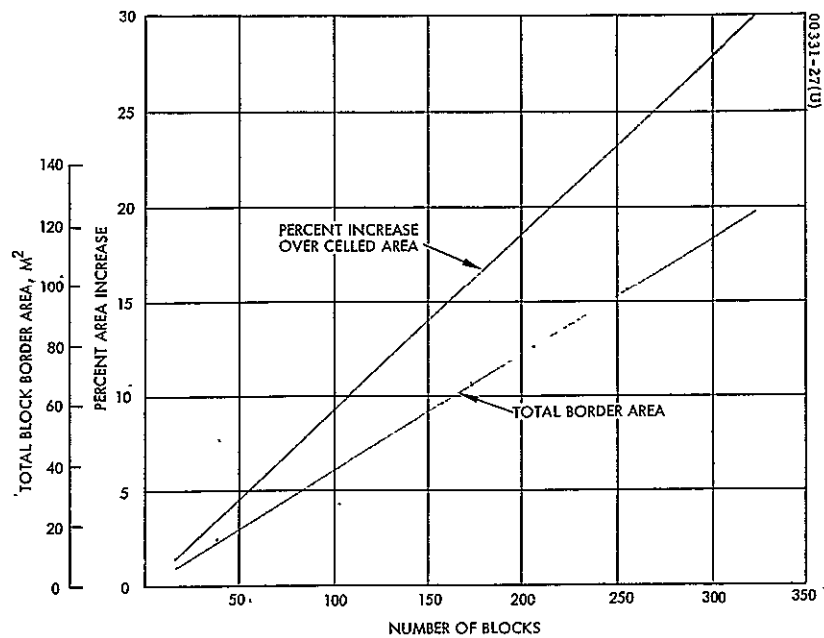


Figure 27. Substrate Area for Block Borders as a Function of Number of Blocks, Specific Approach

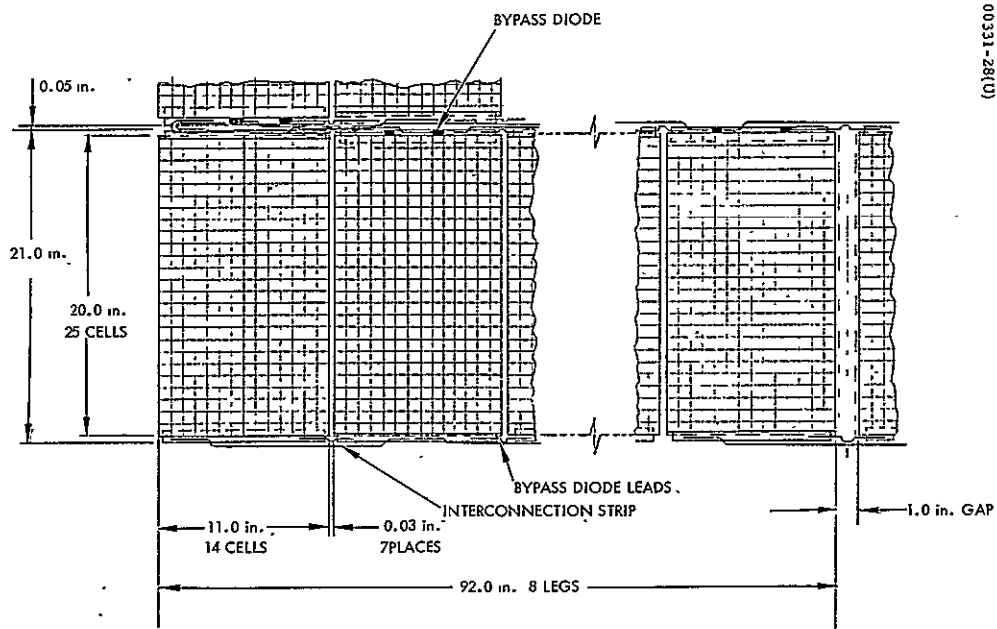


Figure 28. Typical Sector, Specific Approach

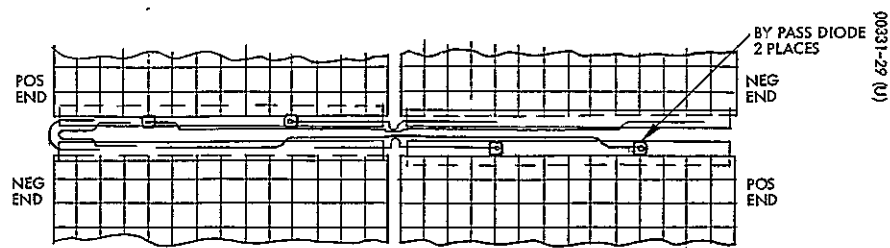


Figure 29. Typical Bypass Diode Interconnection

Each of the four blocks of the specific model panel in Figure 4 is folded the entire length of the panel. The need for buses is completely eliminated. This is one major advantage of the simplified model. For a busless design, area is conserved and the high voltage problems associated with bus configuration are avoided.

The 2.5 cm (1 inch) spacings in the longitudinal direction of the panel are presented out of scale to highlight panel segments. These segments are fabricated separately with full cells and joined together to form the final panel. There are eleven segments for each panel. The segmented layout of the simplified specific model highlights another of its advantages. The segments are basically identical and interchangeable. Such equivalence would allow construction of a spare segment. Fabrication, handling, and testing techniques may be duplicated for each segment.

Figure 27 presents the loss in substrate area due to borders for full length blocks with no buses. Each panel in this design employs four blocks. The penalties for busless design are shown.

Interconnection of blocks through switching as well as regulation is accomplished in a small area at the base of the panel. Regulation leads will be run between the folded halves of the controllable block. Seven of the sixteen, 1 kv blocks are regulated.

A detailed sector of the specific model panel in an unregulated block is presented in Figure 28. All blocks have a full complement of 14 cells in parallel. There are no smaller parallel arrangements as in the universal model. The parallel direction is transverse to the drum axis. This detail drawing may be oriented to the full panel layout by locating the 1 inch gap on Figures 4 and 28; spacing between the folded halves of the unregulated block is 0.13 cm (0.05 in). The sector has eight cell groups connected in series. Each cell group is a basic module composed of 25 cells in series by 14 cells in parallel. The panel segments, spaced 1 inch apart on the panel drawing, have eight such sectors isolated from one another electrically. All spacing on both array models will allow in-air ambient testing.

Employing the principles already developed in the Failure Protection analysis, one bypass diode is used for every 50 cells in series (Figure 29). Since 14 cells in parallel are employed, more than one open cell failure per row is required to enter the bypass mode. The one diode per 50 series cells will keep the failure rate of bypass modules below 1 percent for the 5-year mission. The universal model required one bypass diode per parallel row and a copper strip for diode mounting and heat sinking. This bypass configuration resulted in a 3 to 4 percent area increase for the universal model. However, the specific model with only one diode per 50 cells in series has the diode mounted on the copper interconnect at the end of the cell group. The interconnect will serve as an adequate heat sink. As a result, open protection for the specific model results in no area penalty.

In summary, Figure 4 represents the specific array model for the performance increments at the end of this study.

3.3.3 Conclusions

The two array models have been configured in sufficient detail to allow performance comparison with a base conventional low voltage array.

The very simplicity of the specific model will provide an optimistic boundary for the performance increments. The specific model has no buses, is not penalized by area for open failure protection, and allows simplified fabrication methods. However, the general nature of the universal model will produce a more pessimistic boundary. The two together should bracket the actual performance of a high voltage array in terms of weight and area penalties.

3.4 GENERAL SUMMARY

3.4.1 Design Principles

The basic design principle developed in the first High Voltage Solar Array Study remains unchanged:

Any practical low voltage array can be designed to operate at high voltage with only a minimum of modifications.

Results of the present study have caused no change in this position statement.

Only one design action has been proposed in the solar array area which is not common to conventional low voltage flexible arrays; the back-side conductive grid. The need for such a grid awaits confirmation in follow-on testing.

The present study assumed and built upon the general design principles developed in the first study. The results of the previous study have been employed in the present study. At the same time, duplication of reporting was avoided. Previous design decisions which were used are summarized in Appendix B.

3.4.2 Models for Boundary Development

Two conceptual approaches to array design have been outlined. The universal concept is independent of mission. The specific concept is mission optimized.

A model for each concept has been chosen and configured to allow calculation of performance increments. The specific model is optimistic, the universal model is more pessimistic. Both have been developed to allow the establishment of boundaries. These boundaries should bracket the actual performance of a final design. Both models will be shown in the performance increments at the end of the report.

The primary penalty in the array area is the minimum required thickness of the substrate and coverslide for high voltage design. Both thicknesses are greater than the conventional flexible array with which comparisons are to be made. A method for overcoming this thickness barrier has been proposed: conductive coatings. Since such coatings should allow the use of substrate and coverslide thicknesses comparable to the conventional array, performance increments will be presented for both models, with and without conductive coatings.

In addition, performance increments will be shown for both beginning of life and end of life. End-of-life calculations are based on a 5-year orbit raising mission for the conventional low voltage array as well as the high voltage array.

As has been indicated, both arrays configured above are models. A final design would probably lie between the two models in performance. A key development of this study has been the conception of a method of computer optimization of the array layout for specific missions. It is believed that this approach will be the most fruitful and efficient method of high voltage design. The use of this method will be presented as the conclusion to this solar array section; it is seen as the projected design of a high voltage array.

3.4.3 Projected Design

Computer Design Problem

A major problem which is faced in the design of a high voltage array is that of most efficiently matching the solar cell layout to the mission load requirements. These requirements impact the array in the areas of performance, sequencing, and reliability.

In the area of performance the array must be capable of supplying the correct current and voltage to each load. For the class of missions under present consideration, it has been assumed that the current requirements can be from 0 to 15 amperes and the voltage from 1000 to 16000 volts.

Sequencing of loads is also necessary. This means that the array must not only match several diverse loads, it must be able to be reconfigured to match other, completely different sets of loads.

In addition, reliability considerations necessitate that redundant power be available for critical loads. It is here assumed that loads would be separated into categories of critical and noncritical and that in the event of failure the former would use power normally designated to the latter. In order for this to be possible, a certain number of the blocks associated with the noncritical loads must be interchangeable with those of the critical loads.

The solar array must be capable of satisfying all of the foregoing requirements with maximum efficiency. For a given set of sequencing and reliability constraints the basic cell blocks and the subsequent hard-wiring and switching matrix must be selected to give maximum utilization of area and minimum weight.

Approach

The only really efficient way to design a configuration with these capabilities is to use a computer optimization approach. This has the distinct advantages of flexibility, precision, and low cost.

A computer program is the most flexible means of formulating a design by taking into account a number of complex and simultaneous factors as is the case here. Any input may be varied at will, giving rise to data which can be used in parametric studies of design-mission tradeoffs. Any hypothetical mission or design may be studied.

In selecting block size increments of current and voltage, the precision of the method used is critical to the efficiency of the final design. The iterative capabilities of the computer are perfectly suited to this task; all possible combinations of voltage and current increments, and the effects of their interactions, can be taken into account to produce the most efficient design.

Once the program is written the cost of arriving at a design for a given mission is much lower than by conventional means. The design is arrived at in much less time and subsequent design changes can be made rapidly, thereby reducing schedules and their associated costs. There is, of course, a cost associated with the original writing of the computer program. This is, however, not great when compared with the cost of arriving at an array design for even one mission by conventional methods, and the program can be used for a series of totally different missions.

Present Program

An example program has been written which takes the first steps toward accomplishing these ends. To simplify the task somewhat, the program was limited to using only two increments in current and two in voltage. Under actual design circumstances, the program would select the optimum number of current and voltage increments for the particular set of loads. There were also assumed to be six simultaneous loads and no requirements for sequencing. The present program has the capability of handling any number of simultaneous loads, but sequencing ability would have to be added. This program is presented in Appendix C.

The task of the computer in this program was to determine the sizes in voltage and current of the smallest number of basic blocks needed to come within a given percentage of matching all the loads. This program was run parametrically for a number of different sets of randomly selected loads. Each set of six loads totaled 15,000 watts. Figure 30 has the results of this study showing the percentage of total load requirements met exactly, as a function of the number of blocks required. This percentage of load coverage is determined by taking the weighted average of the quotients of

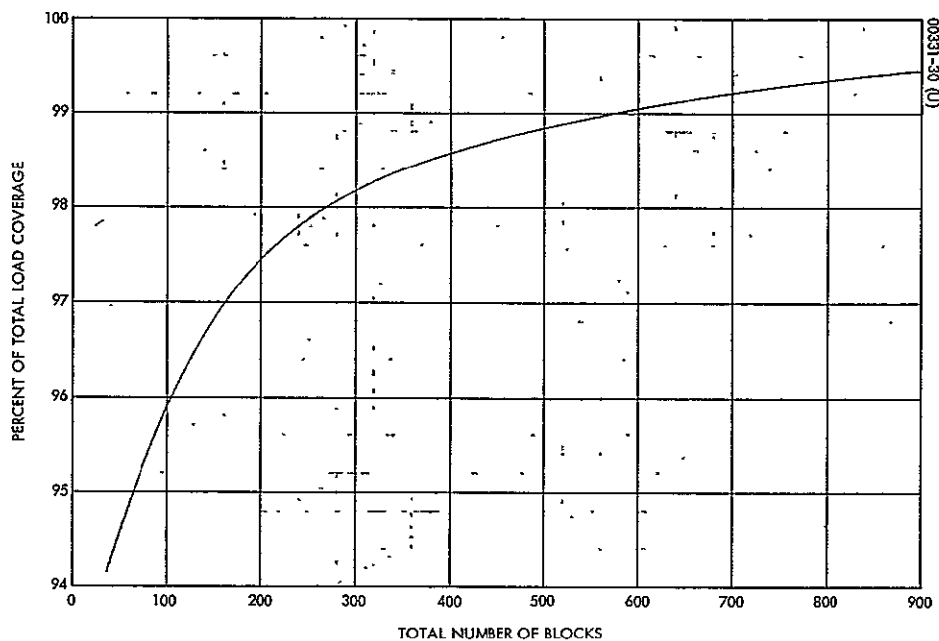


Figure 30. Load Coverage Efficiency as a Function of Total Number of Basic Blocks (Before Hard-Wiring)

the power delivered to each load divided by the power required by each load, i.e.:

$$\text{Percent load coverage} = \left(\frac{\text{Power delivered}_1 + \text{power delivered}_2 + \dots}{\text{Power required}_1 + \text{power required}_2 + \dots} \right) \times 100$$

The solar array would have to be oversized by an amount equal to the power required to make up the difference between the percent load coverage and 100 percent coverage of the loads. For example, a load coverage of 97 percent would require that the array be oversized by 3.1 percent.

Array efficiency can be enhanced further by taking advantage of an additional design approach. It has been found that the number of blocks, and their requisite buses, can be reduced to as little as 25 percent of the number shown if the blocks are hard-wired together on the panel before being connected to their buses. This hard-wiring must include, of course, allowances for sequencing and redundancy requirements.

Other Considerations

The final chosen design will be heavily influenced by fabrication and testing considerations. The combination of large array area and high voltage operation will shift a higher proportion of total costs to the manufacturing sequence, higher than conventional arrays. As a result, the optimum conceptual design will be constrained by testable areas and by required duplication as well as simplicity in fabrication. Additional emphasis should be given to recent developments in pulsed illumination in array electrical tests and in modular cell-group fabrication techniques.

4. REGULATION

4.1 INTRODUCTION

The high voltage solar array approach for providing conditioned power directly to the using load requires unconventional regulation concepts in order to achieve the maximum system benefits in terms of reduced weight and improved reliability.

The power for individual loads can be derived from combined blocks of solar array power which have been sized in voltage and current capability according to the total number of loads and the time sequence during the mission when the separate loads are operative. The combining of blocks to roughly meet the load requirements can be achieved by configuring the blocks (using hard-wiring and reconfiguration switches) into series, parallel, series-parallel, or parallel-series arrangements. The specific arrangement, of course, depends on the load's voltage and current needs and the block sizes. Once the blocks are configured, it is the function of the regulation subsystem to modify the open-loop I-V characteristics of the combined blocks in order to offset load and source variations and to maintain the desired regulation accuracy for either constant voltage or constant current regulation modes. It appears that this fine control can best be achieved by using switches to discretely modify the output levels of given blocks in the combination. Hence, in general, the power source for a load is composed of a combination of controllable and uncontrollable blocks - the I-V characteristics of the controllable blocks being adjusted by activating switches to maintain a fixed output.

The following sections will discuss suggested approaches for satisfying the system regulation requirements and the type of components and subsystems required. A detailed design example is presented to show source and load variations that need to be considered. Techniques for closed-loop operation are considered and suggestions for component location given. The environmental and dimensional considerations for placing electronics on the panel are discussed.

4.2 CONCEPTUAL APPROACHES

Without loss in generality, attention can be temporarily focused on techniques for controlling and regulating a single block of power. Assume that a block of solar array power has a known I-V characteristics and that

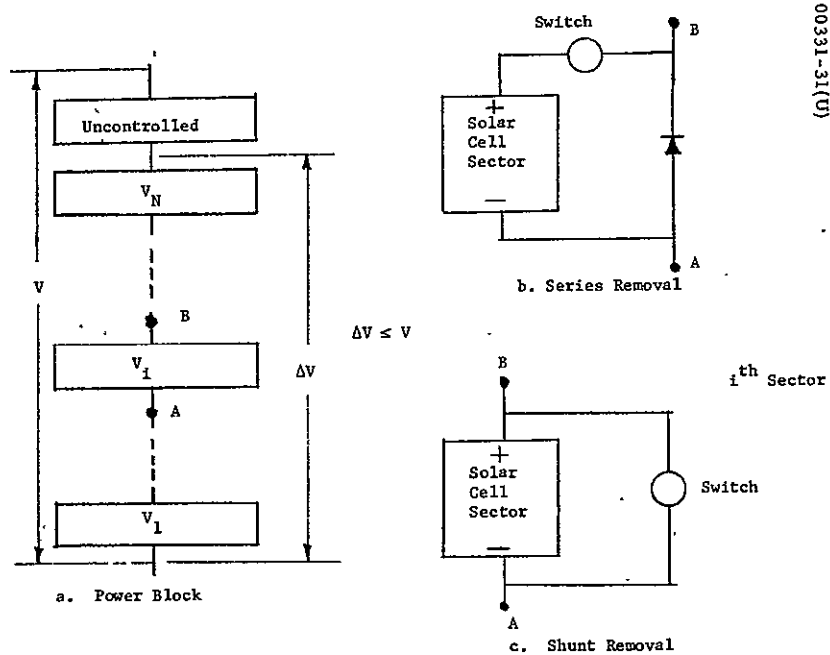


Figure 31. Techniques for Regulation Voltage Removal of Weighted Voltage Sectors Within a Controllable Block

the current capability is sized properly. By straightforward design procedures (to be presented in a later section) the percentage of the block's voltage that must be removed at any time (due to load and/or solar cell output variations) can be determined. Since the maximum percentage to be removed remains constant, the actual voltage removed, ΔV , at any given current level, can also be found. In order to satisfy the regulation specifications, ΔV must be removed in small steps or in a weighted format that produces an equivalent effect. If \bar{V} denotes the step size, then at minimum (load) current, the relationship

$$\frac{\bar{V}/2}{V - \Delta V} \times 100 \leq \eta$$

must be satisfied (for voltage regulation) where V is the total open loop capability at the given current, $V - \Delta V$ is the desired output level, and η is the required percent regulation of the block. In the present study, regulation of ± 0.1 percent for a load variation of ± 10 percent was considered. This translates into ± 1 volt/kv or ± 1 ma/ampere and principally affects the number of digital switches needed for regulation and the accuracy of the voltage and/or current sensing.

4.2.1 Techniques for Voltage Removal

Figure 31a represents a power block of a given current capability, I . Individual solar cell voltage sectors V_1 through V_N which sum to equal ΔV ($\Delta V \leq V$) can be removed by the switch techniques shown in Figures 31b and c.

The series removal technique must have the switch closed to add voltage (power) to the output of the block. When open, the voltage is removed, but the continuity of load current is maintained through the bypass diode. Note that the switch passes the full current when the power is required, hence, any power dissipation in the switch would diminish the useable power of the solar cells. Here, the failure of the switch in the open circuit state would constitute a power failure.

The shunt removal technique clamps the I-V characteristics of each voltage sector to short circuit. The shunt switch is opened to increase the load voltage and closed to reduce the voltage. Since the switch does not pass current when the sector's power is in demand, the efficiency of the regulation schemes using the shunt switching approach is unaffected by the internal impedance of the switching device. An additional possible benefit of the shunt switching approach is that the total block can be clamped to short-circuit even when the shunt switches are inoperative. Also, the nominal current in the shunt switch, when on, is the difference between the load current and the short circuit current of the sector. Typically, the shunt removal technique can be mechanized with switches with much lower current capabilities than the series switch approach. A short-circuit failure of the switch constitutes a power failure.

Comparing the two techniques of voltage removal, the shunt switching scheme is preferred. This scheme is more efficient both from the standpoint of power handling efficiency and drive power efficiency. In addition, if

mechanized with solid-state switches, the loss of drive would not lead to a permanent loss of power.

4.2.2 Weighted Voltage Sectors

A number of voltage weighting schemes have been considered. Let ΔV represent the maximum voltage that is to be removed from a given block with a discontinuity of the transfer characteristic not to exceed \bar{V} . Then for α and n_α integers, the maximum voltage removed by an α -base (radix) regulation scheme can be represented by the equation:

$$\Delta V = \bar{V} (\alpha - 1) \left[1 + \alpha^1 + \dots + \alpha^{(n_\alpha - 1)} \right]$$

where $\alpha - 1$ is the number of sectors of each voltage weighting and n_α is the number of different voltage weightings employed. This class of systems produces typical sector sequences for varying α and $\bar{V} = 1$ as follows:

$\alpha = 2$: 1; 2; 4; 8; 16; 32; ... (binary weighted system)

$\alpha = 3$: 1, 1; 3, 3; 9, 9; 27, 27; ...

.

.

.

$\alpha = k$: 1, ..., 1; k, ..., k; k^2 , ..., k^2 ; ...
(k - 1) times (k - 1) times (k - 1) times

.

.

.

$\alpha = \frac{\Delta V}{\bar{V}} + 1$: 1, 1,, 1 (single weighted system)
 $\frac{\Delta V}{\bar{V}}$ times

The latter sequence removes ΔV in \bar{V} steps using $\Delta V/\bar{V}$ switches. As a point of reference, consider the case of a system where $\Delta V = 511$ volts, $\bar{V} = 1$ volt. The number of switches required with the binary system is 9, while the single weighted system would require 511 switches. It can be shown that for the highest probability of smoothness of regulation and for minimum solar cell power loss without switch redundancy, the single weighted system is best. From a systems standpoint, however, this system is impractical and a scheme based on multiple redundant binary weighted (at least low α) sectors presents an optimum approach for controlling a block of power with a reasonable number of control switches.

Even when limiting the block subdivision to binary formats, a wide range of inblock sector arrangements are possible. Four viable arrangements are displayed in Figures 32 and 33. The principal benefit of current division, as shown in Figure 33, is the reduced current rating required of the controlling switches. The concept of voltage division plus current trimming, also shown in Figure 33, allows the possible sharing of current strings among various controllable blocks where the switching of the strings can be accomplished with reconfiguration switches. This latter concept is closely related to the suggested load regulation approach using controllable and uncontrollable blocks.

4.3 DESIGN EXAMPLE

Before proceeding to the discussion of logic schemes for establishing closed-loop operation and the requirements for voltage and current sensors, a relatively detailed design example will be presented to indicate typical considerations and design procedures for sizing the power and voltage removal portions for a specific load. Although the example considers a load requirement of voltage regulation at 1000 volts and 1 ampere, the procedure is applicable to most levels of voltage and current. Also, since fine current control is to be achieved by voltage removal, the discussion is extendable to current regulation with minor modifications.

Specifications

- 1) Provide 0.1 percent voltage regulation at 1000 volts.
- 2) The 1000 volts shall be near the maximum power point at end of life (i. e., 1000 volts at 1.1 amperes represents maximum power at end of life).
- 3) Nominal load current is 1.0 ampere.
- 4) Load variation is ± 10 percent.
- 5) Source variation is a function of temperature and particulate radiation damage (see Figure 34 and Figure 35, respectively).
 - a) Assume an operational temperature variation of $\pm 10^{\circ}\text{C}$.
 - b) Assume a total integrated particulate flux of 1×10^{15} equivalent 1.0 mev electrons by the end of life.

Approximate Solution to Example

- 1) The first step is to develop beginning and end of mission I-V performance curves, then to label them as shown in Figure 36. Solar array operation throughout the 5-year mission will occur between the two I-V curve limits.

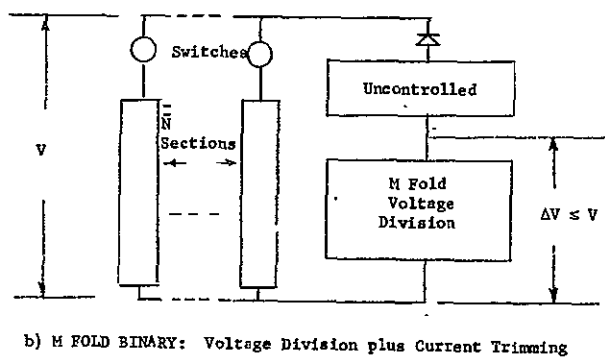
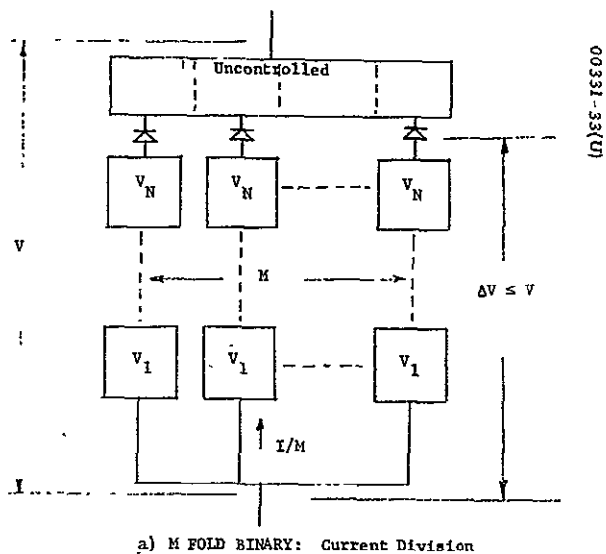


Figure 32. Subdivision of Power Blocks, Voltage Division

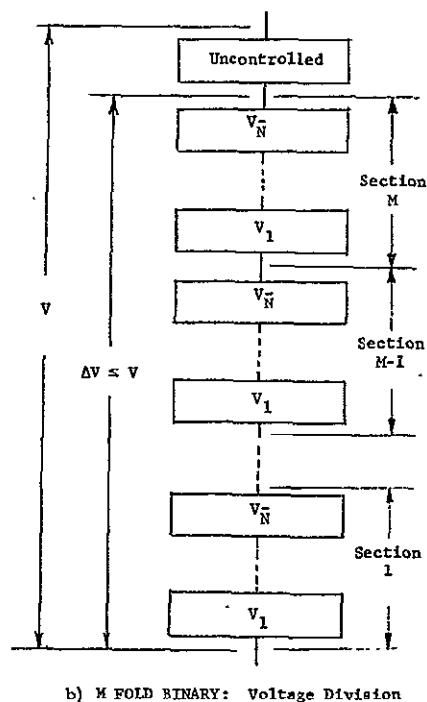
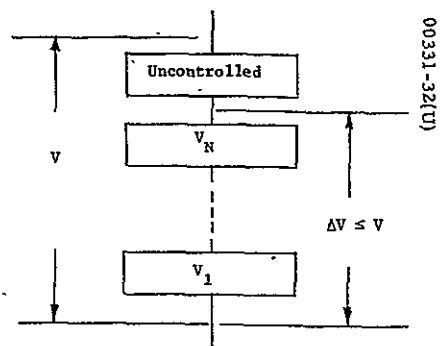


Figure 33. Subdivision of Power Blocks, Current Division and Trimming

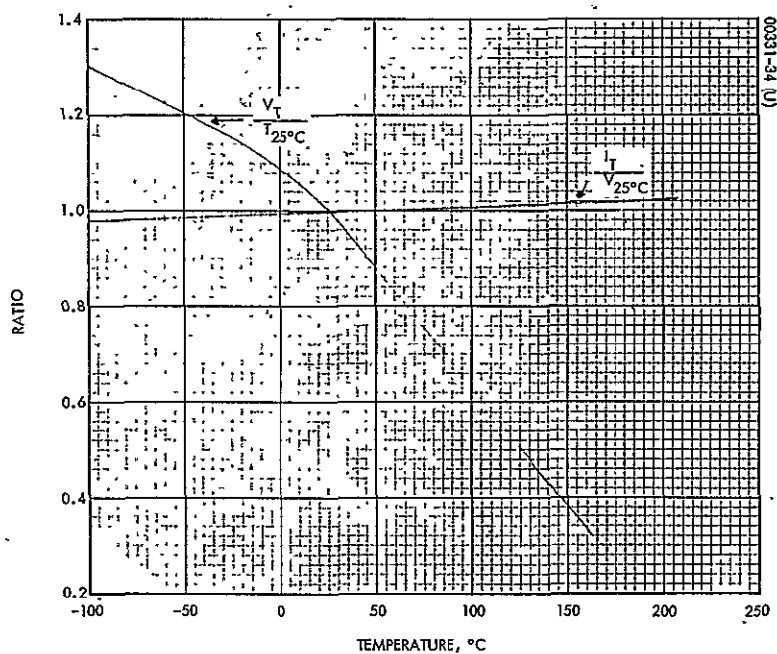


Figure 34. Ratios of Solar Array Open Circuit Voltage and Short Circuit Current (Normalized to 25°C) as Functions of Temperature

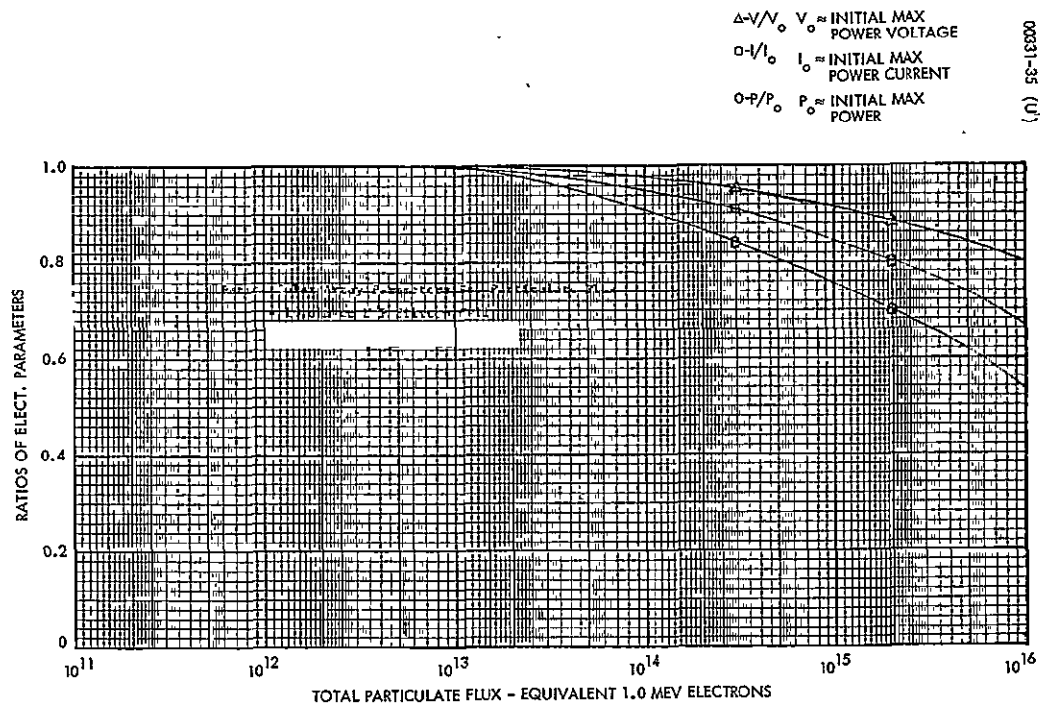


Figure 35. Solar Array Parameter Ratios as a Function of Particulate Flux

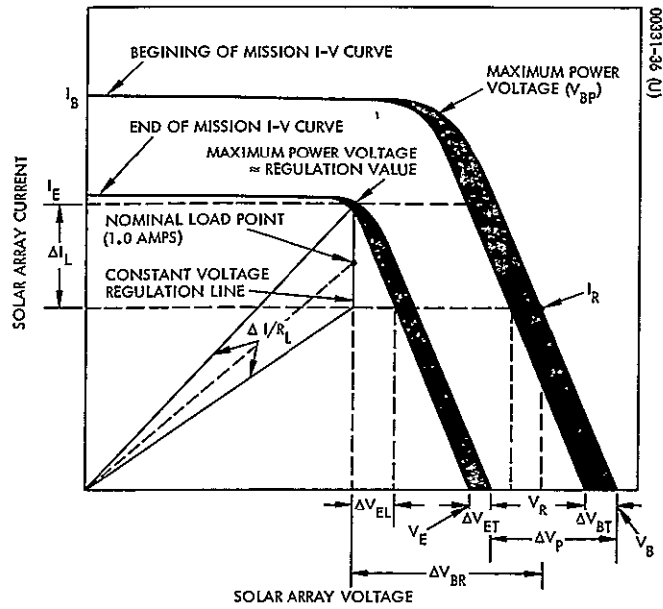


Figure 36. Beginning and End-of-Life I-V Curves for the Design Example

Definitions (see Figure 36)

I_B	=	Maximum short circuit current at beginning of mission
V_B	=	Maximum open circuit voltage at beginning of mission. Occurs at lowest temperature during sunlight part of orbits
ΔV_{BT}	=	Open circuit voltage variation during sunlight part of orbit (beginning of life). Caused by earth's albedo and changes in sun angle
I_E	=	Minimum short circuit current at end of mission
V_E	=	Minimum open circuit voltage at end of mission. Occurs at highest temperature during sunlight part of orbit.
ΔV_{ET}	=	Open circuit voltage variation during sunlight part of orbit (end of life). Caused by earth's albedo and changes in sun angle
ΔV_{EL}	=	Open circuit voltage variation required at end of mission to maintain voltage regulation. Caused by a ± 10 percent change in the load ($\Delta I/R_L$)
$\Delta I/R_L$	=	Variation in load. Given in specifications as ± 10 percent
ΔI_L	=	Variation in load current due to variations in load resistance ($\Delta I/R_L$)
ΔV_P	=	Loss of open circuit voltage during the mission lifetime. Caused by particulate radiation damage
ΔV_{BR}	=	Maximum range of voltage that must be removed from solar array to achieve constant voltage regulation
ΔV_{BL}	=	Minimum range of voltage that must be removed from solar array to achieve constant voltage regulation
V_R	=	The highest value of solar array voltage at the beginning of mission I-V curve that lies within the load regulation load line
I_R	=	The lowest value of solar array current for constant voltage regulation
K_1	=	A constant, the ratio of maximum power current and short circuit current for any solar array
K_2	=	A constant, the ratio of maximum power voltage to open circuit voltage for any solar array

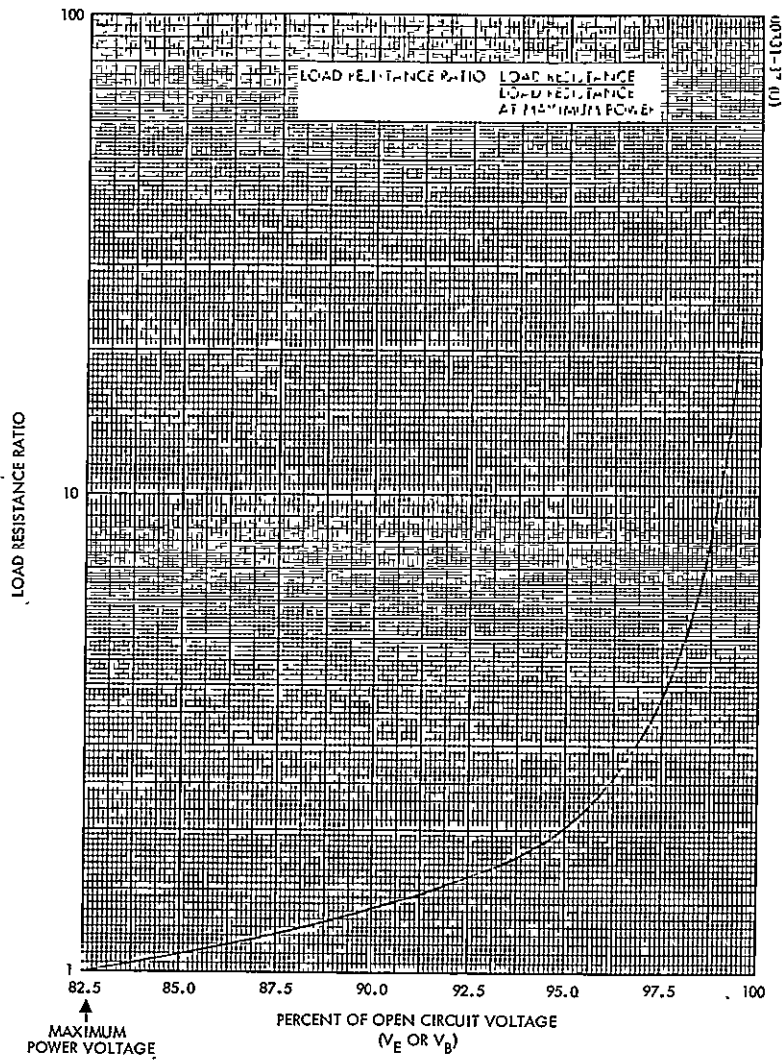


Figure 37. Load Resistance Ratios Corresponding to a Percentage of Open Circuit Voltage

- 2) A reference point is established at the maximum power point on the solar array at end of mission. One side of the load line is drawn to maximum power, the other side of the load line is drawn to a point on the open circuit side of the array. The nominal load point (1.0 ampere) is drawn to a point on the open circuit side of the array. The nominal load point (1.0 ampere) is drawn to the center of the load line ($\Delta I/R_L$) variation.
- 3) From Figure 36, the open circuit voltage (V_E) at end of mission:

$$V_E \cong \frac{\text{Maximum power voltage}}{K_2} ; K_2 = 0.82$$

$$= \frac{1000 \text{ volts}}{0.82} = 1220 \text{ volts}$$

- 4) A good approximation to short circuit current (I_E) at end of mission.

$$I_E \cong \frac{1.0 \text{ amperes}}{K_1} = 1.15 \text{ amperes}; K_1 = 0.87$$

- 5) ΔV_{EL} is estimated from Figure 37. A ± 10 percent load variation in normalized value is 1.0 to 1.2. The nominal load value is 1.1 and occurs at 85 percent of open circuit voltage.

$$\Delta V_{EL} \cong (0.875 - 0.825) V_E$$

$$= 61 \text{ volts}$$

- 6) A value for ΔV_{ET} can be estimated from Figure 34, and Item 5a of the specifications. Assume the temperature variation, $\pm 10^\circ\text{C}$, is centered around 25°C .

$$V_{35^\circ\text{C}}/V_{25^\circ\text{C}} = 1.05, \quad V_{15^\circ\text{C}}/V_{25^\circ\text{C}} = 0.95$$

$$\Delta V_{ET} \cong (1.05 - 0.95) V_E \cong (0.1)(1220 \text{ volts}) = 122 \text{ volts}$$

- 7) Short circuit current (I_B) at beginning of mission is estimated from Figure 35 and Item 5b of the specifications.

$$I_B \cong I_E / 0.84 \cong \frac{1.15 \text{ amperes}}{0.84} = 1.36 \text{ amperes}; I/I_o = 0.84$$

- 8) The value for ΔV_{BT} can be estimated from Figure 37 and Item 5a of the specifications. Assume the temperature variation, $\pm 10^\circ\text{C}$, is centered around 25°C .

$$\begin{aligned} \Delta V_{BT} &\cong (1.05 - 0.95) V_B \\ &= (0.1) (1480) = 148 \text{ volts} \end{aligned}$$

- 9) From Figure 35 the open circuit voltage (V_B) at end of mission

$$\begin{aligned} V_B &\cong (V_E + \Delta V_{ET}) / 0.91; V/V_o = 0.91 \\ &\cong (1220 \text{ volts} + 122 \text{ volts}) / 0.91 = 1480 \text{ volts} \end{aligned}$$

- 10) From Figure 35 the open circuit degradation of (V_B) from particulate radiation. See specifications Item 5b.

$$\Delta V_P \cong (V_B - V_E - \Delta V_{ET}) = 138 \text{ volts}$$

- 11) Assume the load current change (ΔI_L) is a linear function of load resistance change ($\Delta 1/R_L$). With load current changes of ± 10 percent.

$$\Delta I_L \cong 0.2 \text{ ampere}$$

- 12) Assume the solar array current is a straight line function of solar array voltage from open circuit (V_B) to maximum power voltage (V_{BP}).

$$V_R \cong V_B - \frac{I_R V_B (1 - K_2)}{I_B K_I}; \quad I_R = 0.9 \text{ ampere}$$

$$V_R \cong 1480 \text{ volts} \left[1 - \frac{0.9 \text{ ampere} (0.18)}{(0.87) (1.36 \text{ ampere})} \right] = 1280 \text{ volts}$$

13) Maximum range of regulation voltage (V_{BR})

$$\Delta V_{BR} \cong V_R - \text{regulation voltage}$$

$$\Delta V_{BR} \cong 1280 \text{ volts} - 1000 \text{ volts} = 280 \text{ volts}$$

The design procedure above is one method of approximating a solution for the recommended solar array digital regulator. It is meant to serve as a framework for more detailed design procedures. Regulator weighting equations and solar array I-V characteristic equations are adequate to construct a detail design procedure.

Once the power sizing (V and I) and the maximum voltage ΔV_{BR} that must be removed at minimum load current have been determined, and assuming the power or a portion of the power is to be used with other loads in certain phases of the total mission, the load power can be divided into a number of separate blocks. In the design procedure presented here, the power was assumed to be used with a single load throughout the major portion of the array's degradation due to radiation which is typical of the situation for powering an ion thruster for orbit raising.

The sector weighting to achieve the 280 volts of voltage removal at minimum current could take any of the forms previously presented in Figures 32 and 33.

One basic mechanization using shunt removal switching is shown in Figure 38. The sector voltage weighting selected provides for the removal of 286 volts at beginning of life at minimum load current. Normally, redundancy of the lower voltage sections would be provided if the block was to operate alone and ± 0.1 percent regulation was required. Typically, however, blocks operate in parallel and series combinations and redundancy can often be achieved collectively. As should be obvious from this example, as the regulation accuracy is relaxed, the number of switches required are quickly reduced.

The functional blocks represent other portions of the system involved in achieving controlled regulation. These are discussed starting in the next subsection.

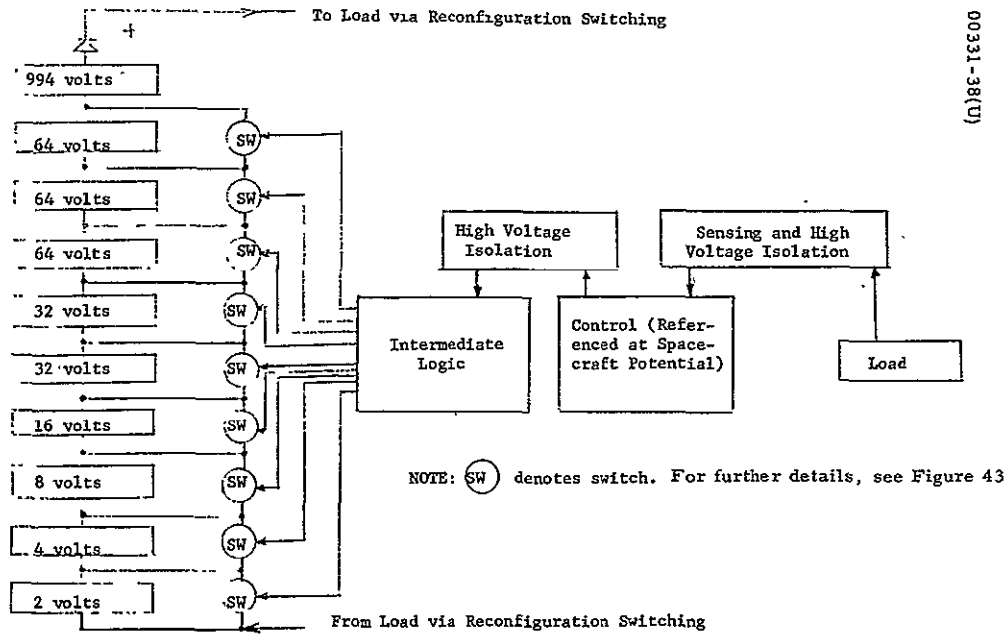


Figure 38. Mechanized Solution for the Design Example

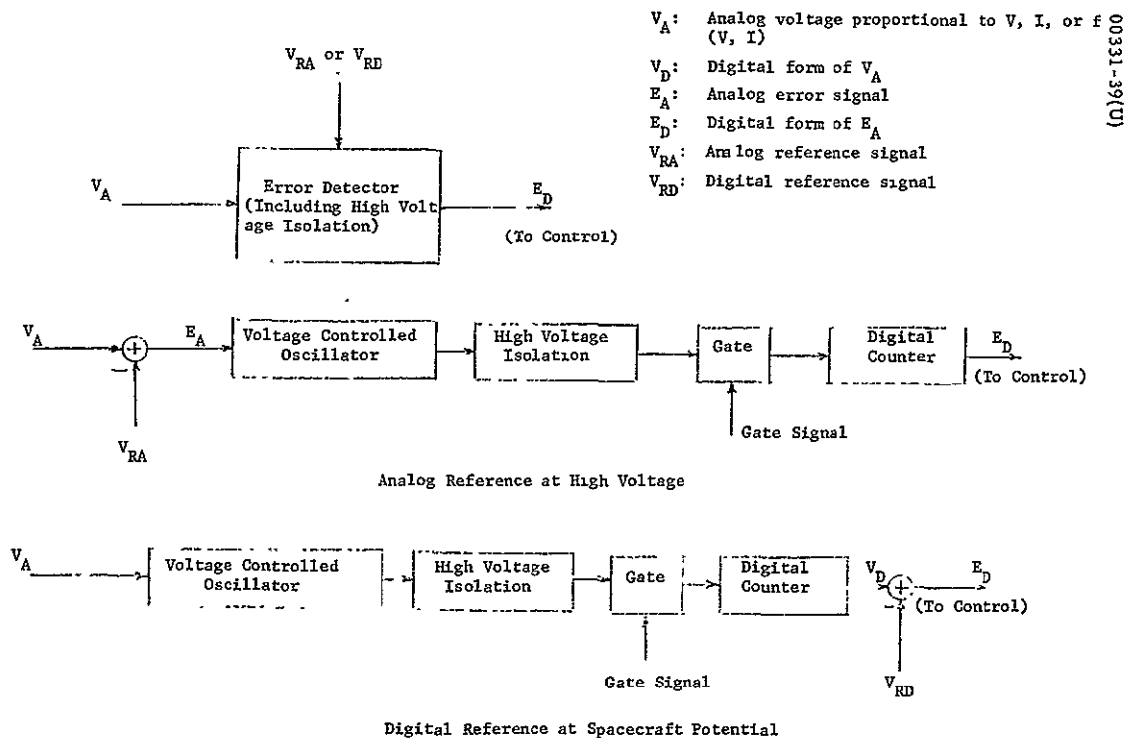


Figure 39. Error Detector, Serial Transfer

4.4 CLOSED LOOP MECHANIZATION

4.4.1 Required Functions

In order to provide load regulation, circuitry (or error detection) in the form of control logic and sensing must be provided in addition to the regulation switches. The function of the control logic is to determine which switches should be activated (opened or closed) on the basis of the error that exists between the sensed output level and the desired level. Because of the regulation accuracy required for some loads, it seems advisable to locate the sensing in-board the spacecraft to minimize environmental variations. The control logic can be totally housed in the spacecraft as a portion of an on-board computer or configured in two sections with the decisional logic in the spacecraft and the intermediate switch drive logic on the panel. The latter approach becomes more desirable as the number of regulation switches are increased. This leads to a minimum number of control lines and points of high voltage interface with the on-board computer.

4.4.2 Sensing and Error Detection

The specific design of the decisional logic format can be relatively straightforward. However, the preparation and transfer of sensing information across an existing high voltage interface represents a major logic system problem. It is projected that the best system approach to minimize this sensing problem is to use an analog-to-digital converter in combination with optical isolation. The converter can transform the sensed analog signal directly into a digital format acceptable to the decisional logic circuitry. The actual conversion can occur on the high voltage side of the isolation with the digital information transferred across the isolation in a series or parallel fashion. Alternately, the conversion can be achieved by a partial and simultaneous operation on the data on both sides of the interface.

Two very general conversion techniques are briefly discussed below. The digital data on the low voltage side of the isolation can represent either the actual value of the sensed output level or the relative error between a reference and the actual value. In this latter case, the sensor would function as an error detector. Basically, either can be considered circuitry for converting analog data (sensed value or error) into a digital form which the control logic can use to make a correction calculation and issue the appropriate digital control signals to the regulation switches. The data used for regulation can be monitored for telemetry and employed to activate protective measures involving clamp and reconfiguration switches.

A Serial Data Transfer Technique

A pulse train with a pulse rate proportional to the actual sensed value or the error is generated by a voltage-controlled oscillator. The wave form is transmitted across the high voltage interface via an optical isolator. A digital counter is gated on for a fixed period. The total count is proportional to the sensed signal or error. This concept is shown in Figure 39.

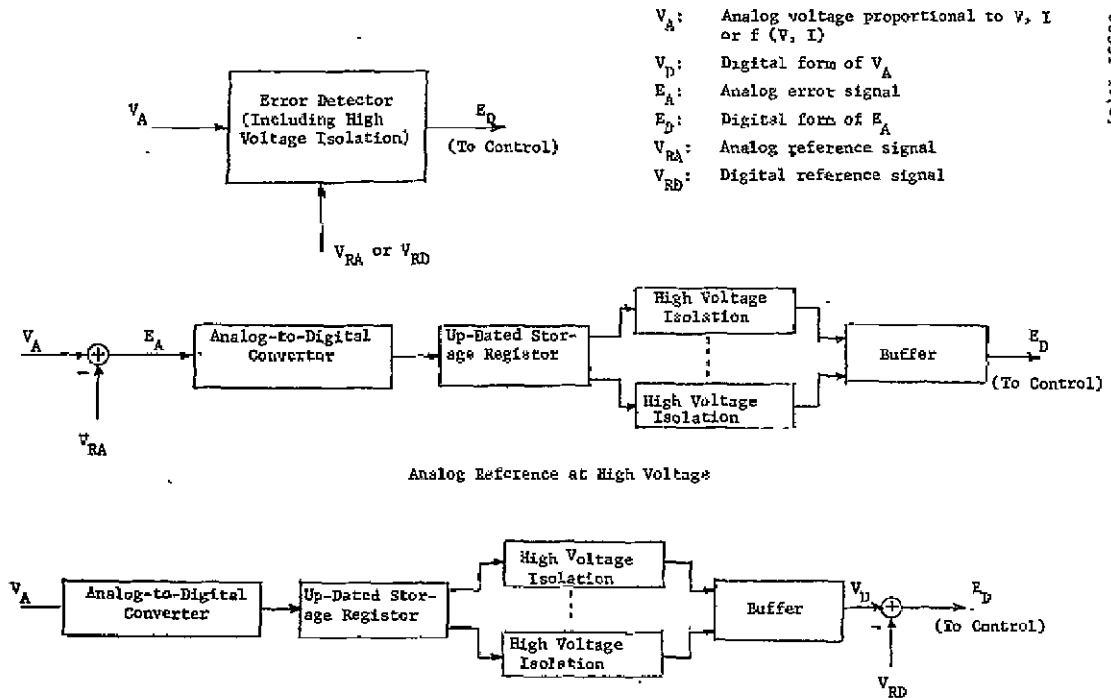


Figure 40. Error Detector, Parallel Transfer

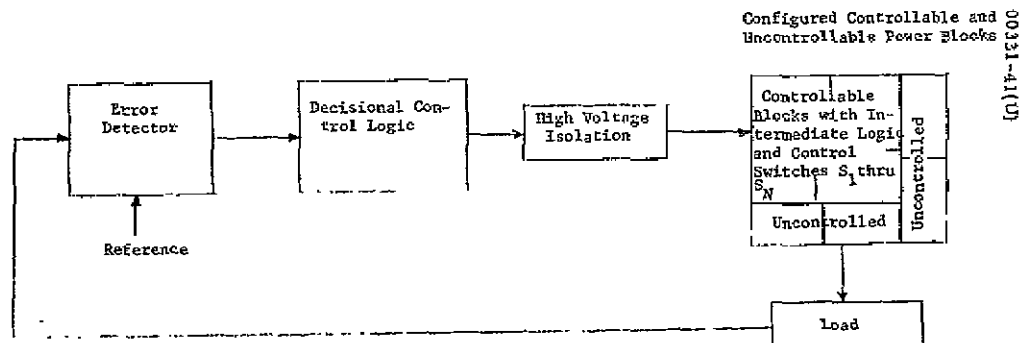


Figure 41. Digital Regulator Block Diagram for a Single Load

A Parallel Data Transfer Technique

The parallel transfer technique is suggested in the cases where the slow response times of the optical detectors restrict the speed of transferring serial data. Any reasonable form of analog-to-digital conversion (ranging from voltage to frequency converter to successive approximation converters) can be used to continually update a storage register situated at high voltage. Each bit of the register, in turn, drives an optical isolator allowing a parallel transfer of the digital data across the high voltage interface. This technique is represented in Figure 40.

4.5 LOOP OPERATION

4.5.1 Single Load

The previous sections presented the major functional areas or parts which comprise the digital regulator approach. The solar array power is sectored, and switches are placed with this power. Hence, the I-V characteristics of the load power are capable of being controlled. The output voltage, current, or a load parameter which is a function of current and/or voltage is sensed (generally in analog form). The data are then converted to a digital format compatible with the logic routine which determines the regulation switches to be activated. High voltage isolation will typically be required in the sensor or error detector circuitry and between the control logic and regulation switches. In general, intermediate logic can be placed with the switches on the panel. In such a configuration the intermediate logic acts as a memory drive circuit for the switches, and its state can be updated with a minimum number of control lines from the on-board decisional control logic. In addition, the high voltage isolation occurs between the control logic and the intermediate logic. The highest voltage stress between the intermediate logic and its regulation switches is then less than or equal to the maximum open circuit voltage of the block of power that the switches control.

A closed-loop block diagram for a single digital regulator is shown in Figure 41. The error detector (or sensor) receives load variations and conditions the data for input to the control. Programmed instructions in the decisional control modify input data as required, and output digital signals instruct the control switches (S_1 through S_N) to open or close. Control switches effectively add to or remove voltage or current increments from the solar array power associated with the given load. Thus, the solar array power output is adjusted until it meets established load requirements.

4.5.2 Multiple Loads

The operation of the single digital regulator described above is an aid to understanding the multiregulator system block diagram shown in Figure 42. This figure represents the total system conceptual approach that is suggested for power regulation of high voltage solar arrays used with multiple loads requiring regulation. The discussion to follow presents one

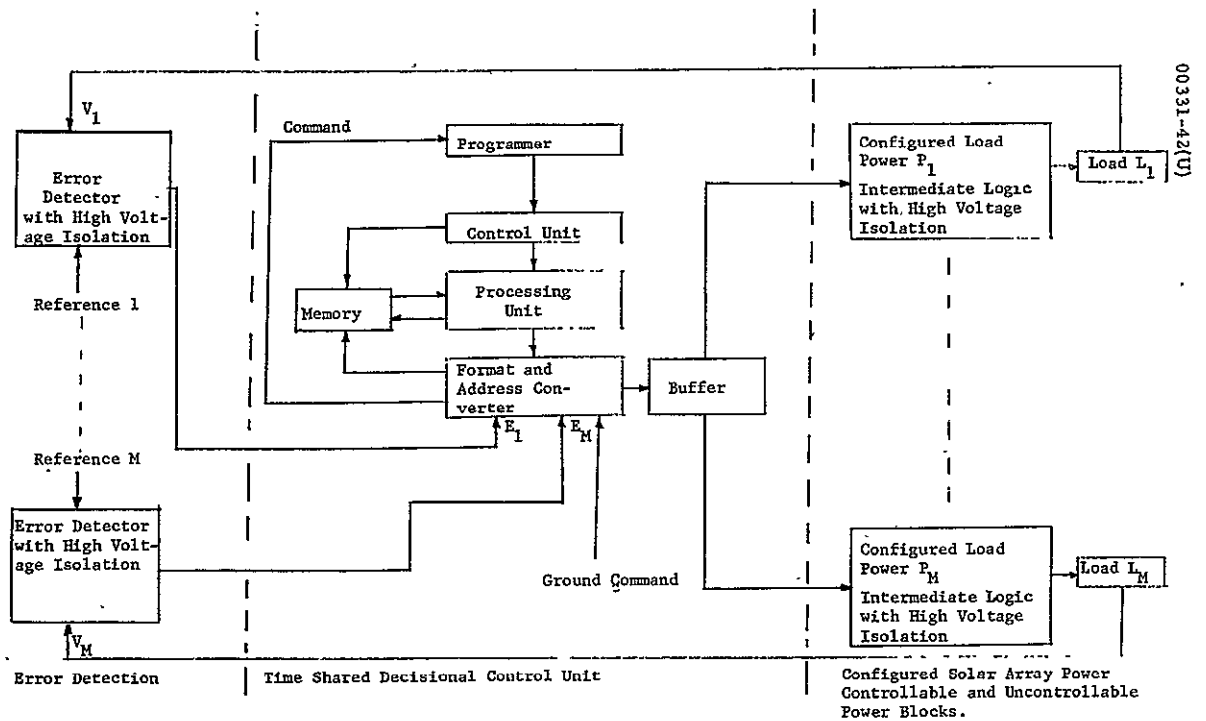


Figure 42. Digital Regulation System Block Diagram

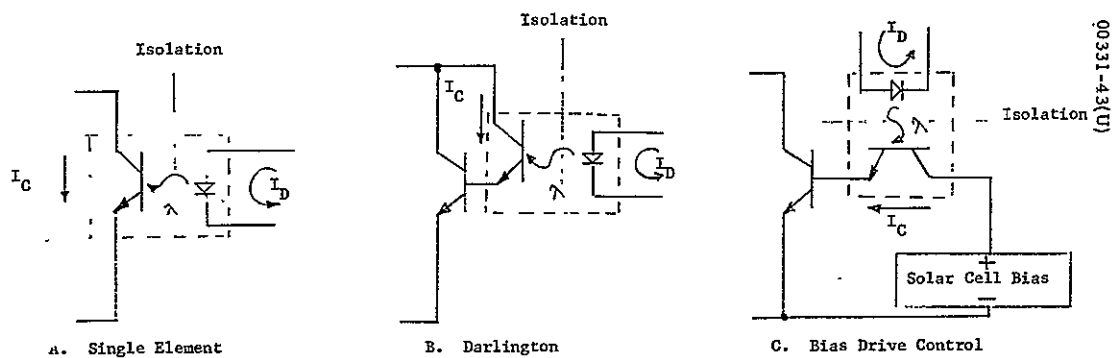


Figure 43. Solid State Regulation Switch Configuration Employing Photon-Coupled Isolation

specific means of logical mechanization, although there are many possible variations on the approach. Symmetry is assumed to exist between the configured load power P_1, \dots, P_M and sensed analog voltages (proportional to V, I or $f(V, I)$) V_1, \dots, V_M . Thus, an operational description for variations at one load and for the correction sequence will suffice for all.

Output variations at L_1 (due to load or source variations) are sensed by the error detector and converted into a digital error signal, E_1 , acceptable for input to the control. A format and address converter (F/A) prepares the error signal E_1 for storage in the memory, and a signal from the programmer to the control unit initiates a digital routine for processing and conditioning E_1 . A control unit signal instructs the memory and processing unit to send the conditioned error data E_1 (now in a form acceptable to the intermediate logic) to the F/A unit. The processed error data are then routed from the F/A to the proper intermediate logic, causing the state of the regulation switches controlling the output to L_1 to be modified.

Ideally, the solar array power has been corrected at the end of the above process. However, weighting changes of the controlled solar cell sector can cause regulation errors due to solar cell failures or radiation damage in the sector. In addition, minor but essentially continuous variations of the load can be expected. Therefore, the regulation process for each load must be iterative, tending to converge toward a zero error signal. It seems desirable to formulate an iterative procedure which would be used by the multiple loops for the various loads. In this case, the decisional control logic could be time-shared (for simultaneous control of multiple loads), and a reasonable amount of control redundancy could be achieved for this portion of the loop with reduced weight and complexity.

4.6 REGULATION SWITCHES

Both mechanical and solid-state devices were considered for fulfilling the switching function of the regulation switches. However, except for packaging problems associated with placing the electronics on the panel, the photon-coupled transistor appears to offer the preferred solution, particularly in terms of the number of required switch operations. As of this writing, the available devices are limited to about 60 volts and approximately 50 ma. The best reported current transfer ratio, I_C/I_D , is approximately two. At least one manufacturer has devices with 2.5 kv of isolation between the photo-transistor and the light emitting (Ga-As) diode. The state of the art in this particular area is advancing rapidly; hence, it is expected that the voltage and current ratings of the transistor and the transistor-diode isolation required for the high voltage solar array could be achieved with a specially designed device.

Figure 43 shows three possible switch configurations that could be used. The appropriateness of each configuration depends on the degree that the voltage and current ratings of presently available devices are extended. Figure 43a represents a single element device capable of switching the total current and of sustaining the total voltage. The limited ratings of available

devices have already been discussed and it is apparent that such a configuration is not now in existence. The Darlington arrangement shown in Figure 43b is a satisfactory way of increasing the current carrying capability, but still requires that the photo-transistor sustain the total voltage; hence, would presently be limited to controlling sectors with open circuit voltages less than 60 volts. The most immediately applicable configuration is that shown in Figure 43c. Here the bias drive current to a power transistor (having satisfactory voltage and current capabilities) is controlled by the photo-transistor. The bias power could be derived from solar cells located adjacent to the solid state switch.

As previously discussed, the regulation switches can be directly driven from the on-board control logic (with a buffer output). This approach requires the isolation at each regulation switch to be in excess of 16 kv; however, some reduction in isolation can be realized by using reconfiguration logic which places the controllable blocks in positions of minimal control isolation stress.

When intermediate logic is placed on the array, the required isolation between this logic and the switches would be less than the maximum open circuit voltage of the controllable blocks of power associated with the given logic. When this design approach is used, the control data signals to the intermediate logic can be transmitted by photo-transistors of the general configuration shown in Figure 43a. This minimizes the number of high voltage interface points for the regulation subsystem.

Typical electrical specifications for either the regulation power switch (any configuration shown in Figure 31) and an intermediate logic drive switch are given below:

Typical Regulation Power Switch Specifications

Collector-emitter breakdown voltage	to 300 volts dc
Current	to 1.75 amperes
Saturated voltage drop at rated current	to 1 volt
High voltage control isolation	16 kv typical (2.5 kv with intermediate logic)
Control power	milliwatt range

Typical Logic Drive Switch Specifications

Collector-emitter breakdown voltage	30 volts dc
Current	10 ma
Saturated voltage drop at rated current	less than 1 volt

High voltage control isolation	16 kv
Control power	milliwatt range

Except for the high voltage control isolation, the electrical characteristics of acceptable switches can have variances from those given. The regulation power switch in particular can have reduced voltage and current ratings. The values listed for this switch are for the specific configuration of 16 identical power blocks (1000 volts at 0.94 ampere, end of life).

4.7 ELECTRONICS ON THE PANEL

When electronic components are placed on the panel, the total packaging must consider both environmental and dimensional aspects. Solid-state logic and regulation switches must be protected from particulate radiation degradation and plasma effects. The components must be packaged to withstand thermal cycling over wide thermal ranges, and there must be sufficient thermal radiating area to reject the internally dissipated power. These factors must be satisfied with a package size compatible with placement on the panel.

The material presented here is also applicable to the solid state, reconfigured switches discussed in Section 5.

4.7.1 Radiation Dose Levels

The radiation dose for solid-state electronic components placed on the panel was calculated for orbit raising trajectories with both 0 and 28.5 degrees inclinations. The dose was calculated for the point at the center of a spherical shield of uniform thickness. Particle spectra used for this calculation included Van Allen protons and electrons and solar protons. The program for deriving the dose levels is an extension of the radiation degradation calculations discussed in greater detail in Appendix A.

The total dose expected at the center of a spherical shield (otherwise unshielded from space) is presented in Figure 44 for the two orbital inclinations. Typical silicon transistors do not degrade significantly with doses less than 10^5 rad (Si). To reduce the dose to 10^5 rad (Si) would require an equivalent spherical shield thickness of approximately 0.33 cm (130 mils) and 0.22 cm (87 mils) of aluminum for orbital inclinations of 0 degree and 28.5 degrees, respectively. Since the dose through a spherical shield is typically more severe than for other geometries, the indicated dose is considered to be a conservative estimate. Shielding materials such as tungsten allow a greatly reduced shielding thickness. For a planar geometry, a tungsten shield thickness less than 0.05 cm (20 mils) per side should be adequate for most components and orbital contingencies. In this case, the maximum contribution of the radiation shielding to the packaging build height would be under 0.1 cm (40 mils). This height contribution should present no difficulty in sizing component packaging for placement on the panel.

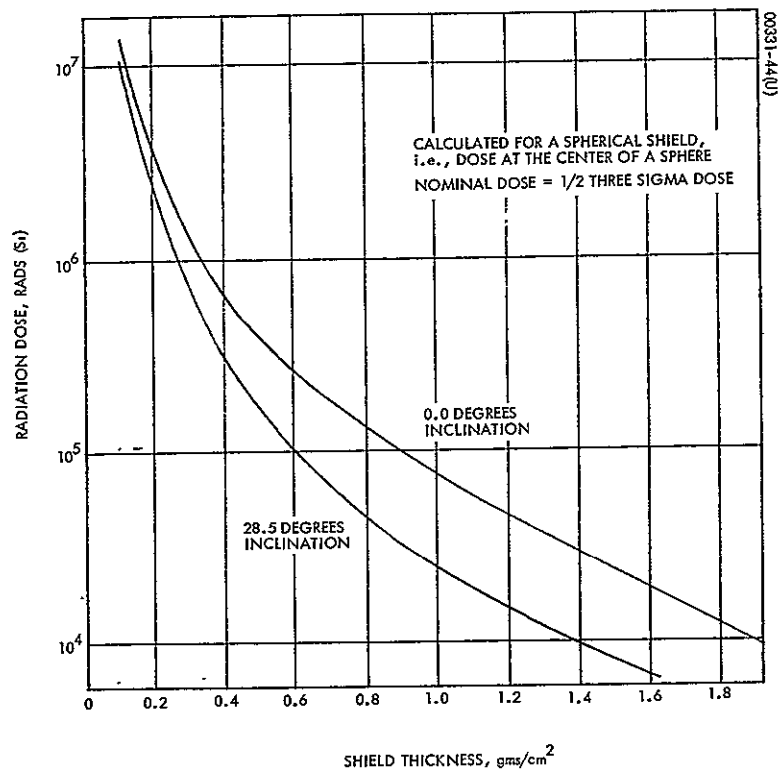


Figure 44. Total Mission Dose From Van Allen and Solar Radiation as a Function of Shield Thickness, 0 and 28.5 Degree Orbit Inclinations, $+3\sigma$

4.7.2 Thermal Considerations

The thermal variations of the electronics placed on the panel will be extreme without active thermal control measures. Required packaging geometries lead to low thermal capacity; hence, if no electrical heating of components is employed, the lower thermal extreme approaches that of the solar cells, -180°C for a maximum duration eclipse at synchronous altitude (see Figure 16).

The packaging used will probably follow hybrid techniques, using discrete chips and often complete integrated circuits, particularly for the regulation concepts with intermediate logic. The materials for construction and the construction techniques will have to be carefully chosen to assure integrity of mechanical interconnections during thermal cycling. The integrity of the chips, on the other hand, should pose no problem, since the lower temperatures will basically be the storage temperatures for the devices. As presently envisioned, system operation will not require the solid-state devices to be operational until a reasonable thermal equilibrium has been reached after exiting eclipse. If the packaging technique is found to produce unreliable interconnection, or if the solid-state components must operate while exiting eclipse, a means of heating the electronics with stored electrical energy may have to be used. Although this latter requirement has only been briefly considered, the general conclusion is that the use of electrical heating is an undesirable complexity and would tend to nullify the advantages of placing portions of the electronics on the panel.

The upper thermal extreme can be controlled by passive means by providing sufficient thermal radiating area to reject internally dissipated power. Thermal radiation areas for electronic packages are discussed in greater detail in Appendix D. Of the various packaging configurations considered, it appears that the least solar panel area will be taken up if the electronic packages use quartz mirrors on the solar illuminated exterior and aluminized kapton on the non-solar illuminated exterior. The thermal radiating area required for such a package to maintain an operating temperature of 70°C at 500 km (270 n. mi) is approximately 13 cm^2 per watt of internally dissipated power. Considering the projected dissipation of solid-state components on the panel, the above area requirements should not conflict with any of the component dimensional restrictions.

4.7.3 Plasma Considerations

Packaging of electronics on the array must use the general principles developed for array design in the plasma environment (Reference 1). Special concern has been shown for dielectric surfaces on the panel. Such surfaces have the potential for high charge buildup due to plasma leakage. The optimum package for thermal control uses a dielectric overcoated mirror. As a result, a dielectric surface is presented to the space plasma.

Such a configuration creates the potential for through dielectric failures to the solid state devices. Whether such breakdown is due to vapor arc formation or Paschen breakdown in overcoat and potting voids, design

compensation is required. The use of conductive coatings already proposed for other array surfaces is recommended. Such coatings, conductive or semiconducting, will allow the surface charge to bleed off and will eliminate the potential for through failures. If it is shown in future tests that failures through the mirror overcoat are acceptable, the mirrored surface itself may serve as the conductive coating. However, if such failures are destructive mechanically, one of the existing transparent conductive coatings will be applied to the mirror's outer surface.

An additional plasma consideration for the packaging is the outgassing of interior potting compounds. A combination of proven techniques will preclude the development of Paschen type breakdown following insertion of the array into orbit. First, venting techniques will be used. Second, vacuum bakeout during the fabrication of the units is suggested. Third, epoxies are preferred as the encapsulant. Although epoxies are avoided on the array surfaces as encapsulants, they are chosen for a closed, vented system. Finally, an initial outgassing period in space prior to initial array turn on will be used.

Control of plasma effects upon electronic packaging is within the present limits of fabrication technology.

4.7.4 Dimensional Considerations

This section presents basic guidelines concerning dimensional restrictions that should be followed in sizing components placed on the solar array panel. Although these guidelines were developed for rollup flexible arrays they also apply in a less restrictive sense for flat, stowed flexible arrays. The restrictions represent engineering judgements on the package sizes that can be accommodated without creating a major problem in the areas of deployment, cushioning, stowing or panel construction. References to component lengths and widths correspond to dimensions in the direction of the long and short sides of the panel.

- 1) Electronic components which are less than 2 cm in length (of any width which can maintain their mechanical integrity) may be up to 0.25 cm thick if mounted on the solar cell side of the substrate.
- 2) Electronics with lengths to 2 cm and thicknesses ranging from 0.25 to 0.65 cm should be arranged in rows over the full panel width. Edge cushioning should be incorporated as an integral part of the packaging.
- 3) Electronic packages with lengths greater than 2 cm definitely required added cushioning and should be avoided.
- 4) Substrate gaps between solar cells and electronic components should be greater than 0.32 cm to minimize binding.
- 5) Components with thicknesses greater than 0.65 cm should be placed on the sides of the panel outside of the cell area, placed

in indentation in the drum, or placed at the inboard end of the panel and deployed from indentation in the drum. The latter approach has been used to house accelerometers.

The above guidelines place minimal restrictions on the components proposed to mechanize the regulation subsystem, since the thermal, particulate radiation, and plasma environmental constraints should lead to packaging sizes with less than 0.65 cm build heights.

4.8 SUMMARY CONCLUSIONS

The power for individual loads can be provided by combining hard-wired blocks. It is suggested the combination be composed of controllable and uncontrollable blocks and that the I-V characteristics of the controllable blocks be adjusted by activating discrete switches to maintain a desired fixed load voltage or load current output.

The preferred candidate to perform the discrete switching function would be the photon-coupled transistor. The switches would be placed on the array with the sectors of solar cells that they control. The major problem in doing this is the range of thermal extremes which the devices will encounter and is an area requiring further study.

In addition to the regulation switches, control logic is required to determine which switch should be activated on the basis of the error between the sensed voltage and current levels and the desired levels. It is proposed that intermediate drive logic (with its own solar cell bias power) be placed with the switches. This logic would be updated by an onboard computer. Such an approach reduces the number of high voltage interfaces.

It is suggested that voltage, current, and load parameter sensing requiring high voltage isolation be achieved by a sensor with photon-coupled isolation and that the sensor perform an analog-to-digital conversion on the sensed data when bridging the high voltage. This digital transfer would nullify the possibility of sensor error due to variations in coupling efficiency. The digital data could then be used directly by the decisional control logic. The data for error sensing can also be used for telemetry, reconfiguration verification and to initiate dynamic protection measures.

The total regulation subsystem can be viewed as a multiple loop digital regulator, one loop for each regulated output. Except for the thermal extremes and the high voltage isolation for issuing control signals and sensing, the design of the regulation subsystem should be relatively straightforward. The layout of the control leads will require special care to minimize electromagnetic coupling with the power bus. Such problems should be resolved with breadboard experiments.

Weight penalty estimates for regulation of the array models, configured using combinations of controllable and uncontrollable blocks, range between 0.25 kg/kw (0.6 lb/kw) and 0.45 kg/kw (1 lb/kw). (More details

on these estimates can be found in Section 6.) Regulation efficiency should lie between 99 and 100 percent for the shunt removal technique of voltage removal. Regulation accuracy to ± 0.1 percent should be possible, the determining factor being sensor accuracy.

The major problem areas are high voltage isolation for control and sensing, thermal extremes for electronics on the array, and sensor accuracy. Future effort should be directed toward evaluating breadboard models of the regulation concepts to determine performance and refine component specifications. Design development studies for the regulation switch and sensor should be undertaken. Fabrication techniques for packaging of the switches and intermediate logic need careful attention.

5. RECONFIGURATION

5.1 INTRODUCTION

The reconfiguration subsystem is considered to be composed primarily of switches and the necessary control electronics to assure that blocks of solar cell power are combined in an acceptable predetermined manner and routed to the appropriate loads. The combining of power blocks can follow a series, parallel, series-parallel, and/or parallel-series format. The routing may be an integral part of the combining process or a separate switching function which connects sets of power blocks which have been combined as required to the load bus.

The investigation of reconfiguration concepts has ranged from relatively complex schemes, which are capable of a high degree of flexibility in combining and routing, to schemes which are essentially devoid of options in their combining and routing process. This approach has provided a basis for uncovering most switch and switching requirements and associated problems which are prevalent with the high voltage solar array.

The reconfiguration subsystem operates on the total power available from the array; hence, failures of any portion of the subsystem can cause a decrease in the power capability of the total system, since array power which cannot be applied to the loads is useless. In general, both the switches and the arrangement in which they are used will determine the probability of success (or reliability) of properly transferring the power to the loads.

An additional power control phase, which is closely tied to that of reconfiguration, is dynamic protective switching or the ability to provide a clamp to the solar array power to minimize and control post-eclipse high voltage stresses, other overvoltage, and over-power conditions. As the discussion progresses in the separate sections, an attempt will be made to show the many apparent advantages of providing an array clamp on a local basis, at each hardwired block of power. The alternative to providing a clamp generally is the requirement that the power blocks be reconfigured to a reduced voltage stress condition, a complete disengagement of the blocks.

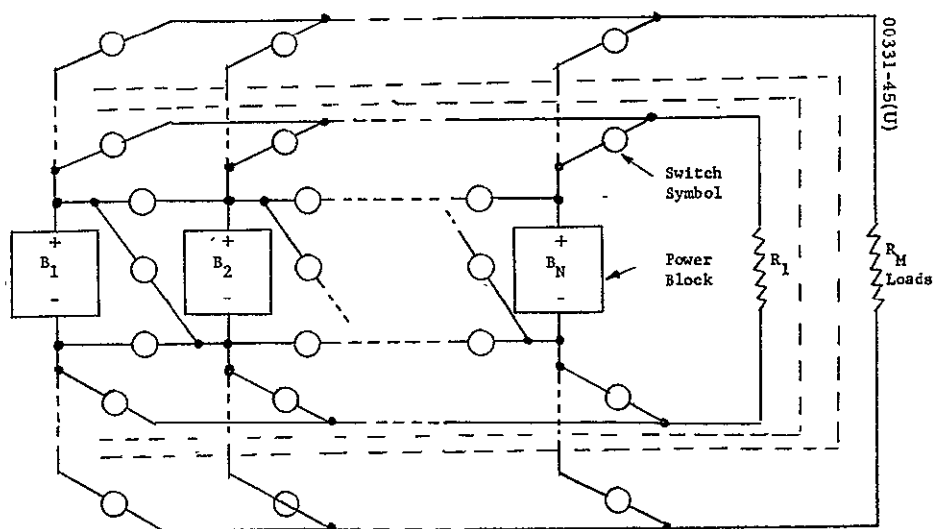


Figure 45. Modified Crosspoint Array

5.2 RECONFIGURATION SWITCHING ARRANGEMENTS

The principle functions of the reconfiguration arrangements can be practically separated (although still interrelated) into the following two duties:

- 1) Arrange basic power blocks into series, parallel, series-parallel, and/or parallel-series combinations commensurate with the number and magnitude of the output levels desired.
- 2) Connect (or route) the output levels to the appropriate loads.

In addition, it is possible to consider certain secondary actions that the switching arrangement could undertake separately (or with the inclusion of clamping switches), such as:

- 1) Provide a clamp for the solar array to minimize or eliminate overvoltage stresses when exiting from eclipse.
- 2) Provide load protection by either disconnect or crowbar action.

Much of the early work in this study was directed toward investigating switching arrays which had their foundation in the well-established field of switching theory. While this may border on the impractical, it does explicitly represent, conceptually, the potential of the high voltage solar array approach. The switching arrangement shown in Figure 45 depicts one of many generalized switch layouts for providing power to up to M loads simultaneously from N basic building blocks. This particular configuration may be classified as a variation of the classical crosspoint array. No a priori knowledge of the output magnitudes desired or the blocks that will be operative to provide these outputs has been assumed. If a polarity reversal of the load voltage during the mission is required, this can, in general (for $M < N$), be most economically provided by reversing the leads to the load.

The number of switches in the switching array shown is given by

$$N_s = 2 M \cdot N + 3 (N-1). \quad (1)$$

The term $2 M \cdot N$ is the number of switches associated with the crosspoint array when each load has an independent return. The factor $3 (N-1)$ corresponds to the number of switches required to provide all possible parallel and/or series combinations and groupings of N blocks. The present configuration assumes that the basic blocks are placed in series by a unidirectional switching format.

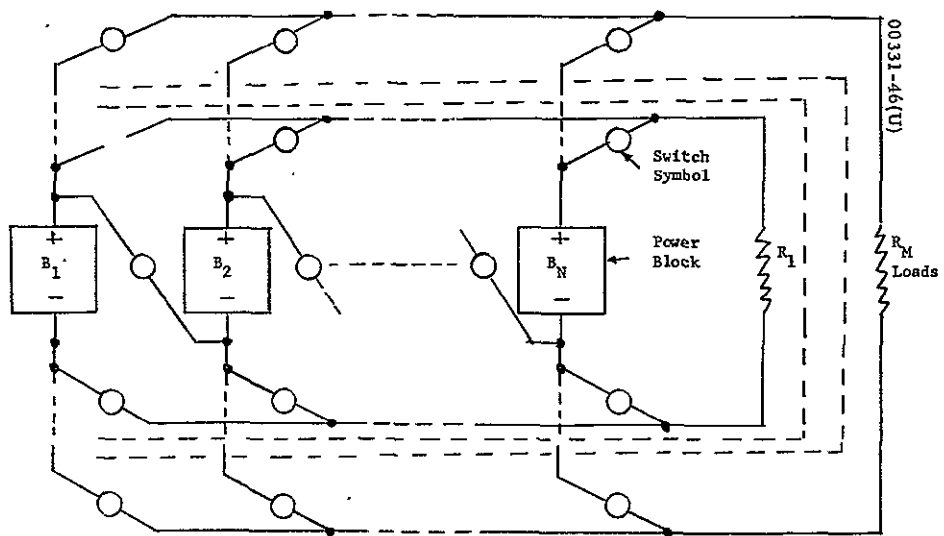


Figure 46. Modified Crosspoint Array Without Parallel Series Capability

Under the constraints of specific load requirements (known and fixed), the number of switches can be drastically reduced; however, care must be taken to recognize that what may at first be considered excessive switching versatility (or flexibility of combining and routing) can, in actuality, be the redundancy required for successful mission completion.

In general, with each prescribed set of constraints, a range of values can be determined for the number of switches which maintain the same array type. As an example, when all loads have a common reference (e.g., spacecraft ground), Equation 1 becomes:

$$N_s = K \cdot N + 3(N-1) \quad (2)$$

where K is dependent on the desired output levels (hence, dictates the format of parallel and/or series combinations) and falls in the range:

$$M \leq K \leq M + 1.$$

For the conceptual high voltage array taken as an example of the specific design concept, there are 16 identical blocks (1000 volts and 0.94 ampere each at end of life); hence, $N = 16$. With $M = 6$, the number of switches indicated by Equations 1 and 2 are:

Equation 1: $N_s = 237$

Equation 2: $141 \leq N_s \leq 157$

The general form of the above switching arrangement has a large degree of versatility or flexibility of combining and routing the various units of power B_1, \dots, B_N to the loads. One of the major drawbacks, especially from the standpoint of mechanization, is the current buildup in the switches in the center core, which provides parallel-series combinations of power with current outputs higher than that provided by a single block. By eliminating the paralleling switches in the center core, the switching arrangement shown in Figure 46 is achieved. In this arrangement, the logical sequence of events to get parallel-series combinations is to first series the blocks and then to connect the series strings in parallel to the load bus. This latter logical sequence has eliminated the current buildup problem; the output to the M loads can still be as varied as with the modified crosspoint array, yet the maximum current in any reconfiguration switch would be the maximum short circuit output current of any one of the blocks, B_1, \dots, B_N . This change in recombination logic greatly limits the range of ratings required of the reconfiguration switches.

The above arrays and their many simplifying modifications have some major limitations when investigated for failure modes, particularly the large percentage of total power that could be lost with a single switch failure. In

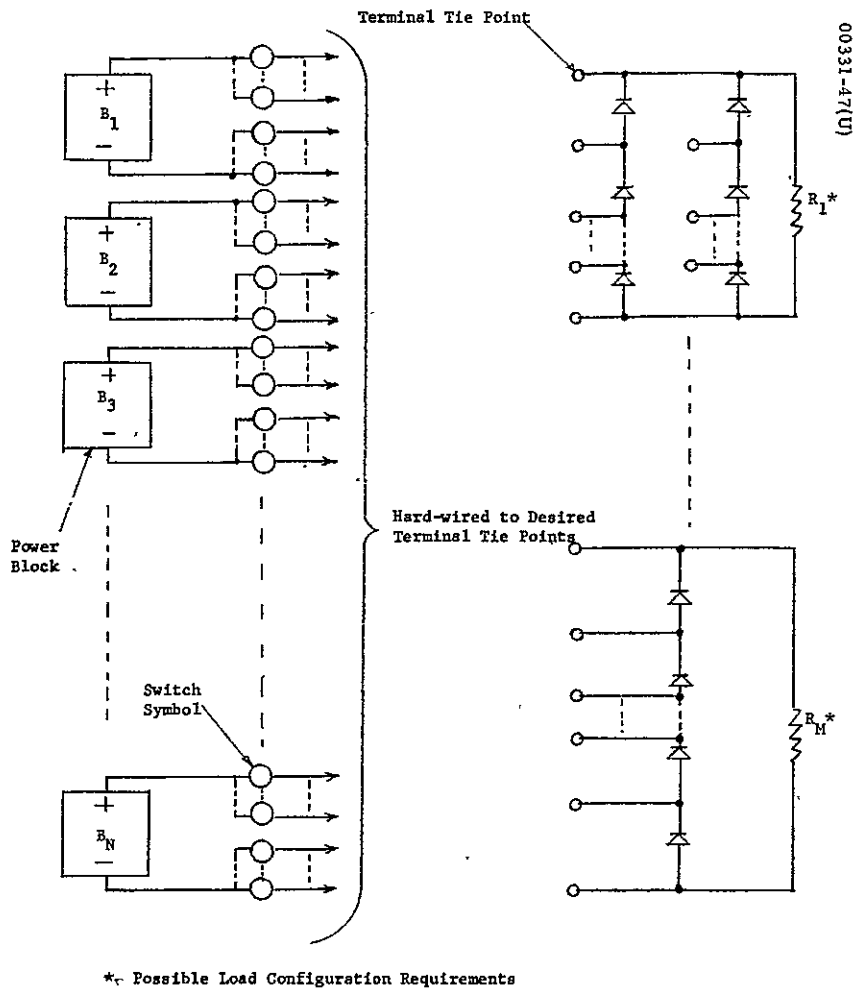


Figure 48. Specialized Reconfiguration Arrangement

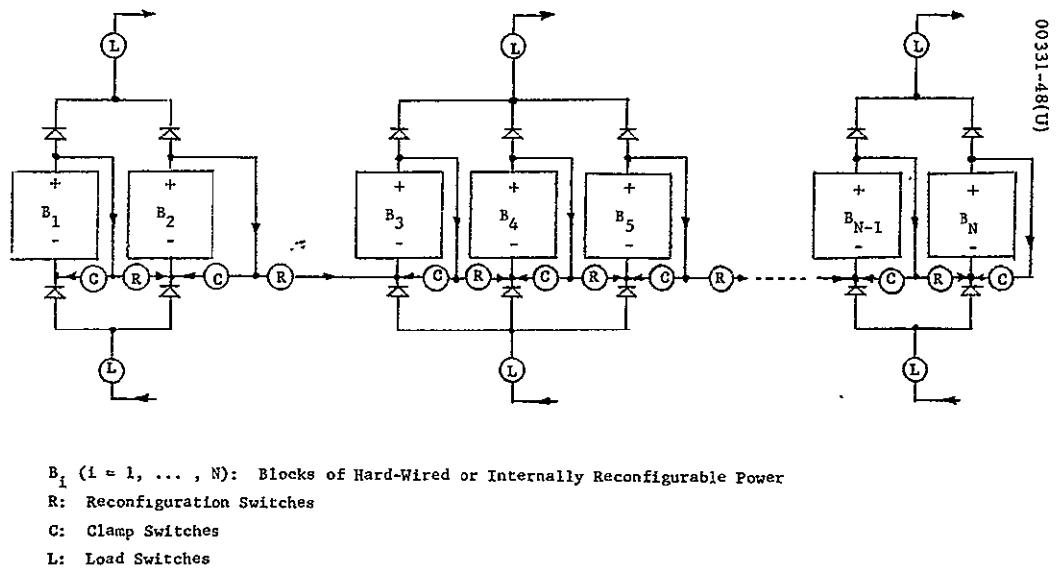


Figure 47. Preassigned Array

light of this, methods of arrangements which are less versatile but which have less catastrophic failure modes (e.g., less worst-case power loss/switch failures) are to be preferred. An example of such an array is given in Figure 47. It has been termed the pre-assigned array, meaning simply that blocks of power (not necessarily identical in either voltage or current ratings) are pre-assigned to be switched to certain load locations as a function of mission time, degree of degradation, switch or power failure at other locations, etc. In general, each block of power will have four or more switches corresponding to two or more locations where the power from a given block can be used. For each load, an arrangement of bypass diodes is configured, and the outputs of the switches associated with the power blocks are connected across the bypass diodes. The diodes provide continuity of load power in case a switch opens and, in addition, provide points where standby or excess power can be switched to provide redundancy. If sufficient location options are provided to the blocks, an open switch would not constitute a failure. In fact, with this class of array, the only true failure (causing a loss of power utilization) is the shorting of a block of power to a load location by a shorted switch, where power is no longer required and where connecting the block to an alternate load would cause the bypass diodes to be forward biased. The current rating of each reconfiguration switch should be equal to the short circuit current of the block with which the switch is associated. Also, for this class of array, there are always two forward voltage switch drops to be considered when determining the power efficiency of the reconfiguration arrangement.

To this point, the reconfiguration arrangements have relied (except for the bypass diode of the pre-assigned array) totally on switches to provide the block manipulation to change voltage levels. These switches have been denoted in an abstract sense to represent either solid-state or mechanical devices. Except for the current levels, the switch requirements (blocking voltage, high voltage control signal isolation, etc.), are much the same for the three arrangements. Of course, an unlimited number of special switch arrangements can be displayed. Each could offer some particular benefit in minimizing the switching complexity and maximizing the reliability for some subdivisions of solar array power and sets of load requirements based on the number of loads, the individual power levels, or the sequences of operation.

A variation on the reconfiguration arrangements previously presented is shown in Figure 48. This specialized arrangement employs power steering diodes to minimize the required number of switches and associated high voltage control signal isolation. This arrangement explicitly displays switches, all of which contribute to the control of the configuration, but which have been functionally separated into reconfiguration switches, clamp switches, and load switches. Again, following the general underlying format of this configuration, it is possible to generate a large family of arrangements for specific load requirements and solar array subdivisions. The major point to be made is that the use of power diode steering techniques can reduce the number of switches required as well as the electronics, control line, and high voltage isolation associated with each switch. In general,

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SW: Reconfiguration switches in any state.
B: Hard-wired power blocks.

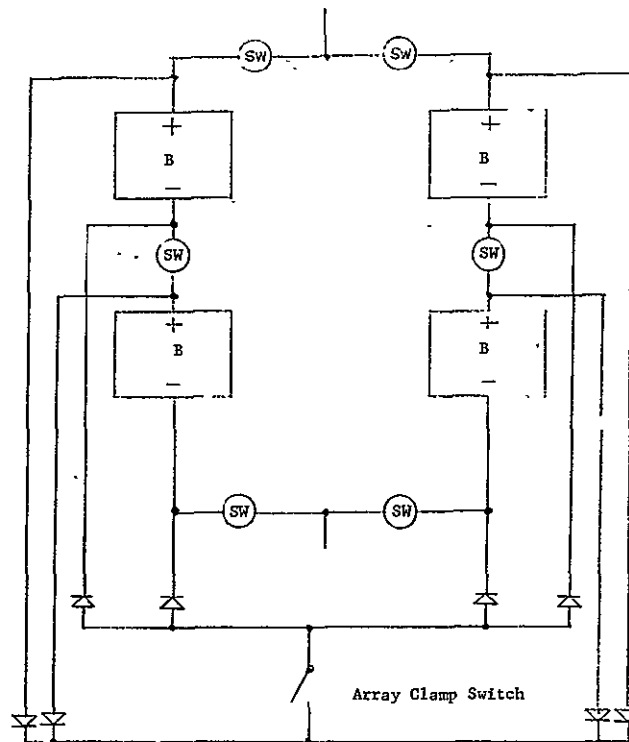


Figure 49. Diode Matrix Clamp

such an approach is most beneficial for the more simplified uses of the array power and for arrangements which use the power at low voltage at the beginning of the mission, when the drop in the power steering diode occurs during the period of excess array power capability.

5.3 ARRAY CLAMPING

The terminology, array clamping, relates to any mechanism which can be used to short-circuit the solar cell array power, and which causes short-circuit current to be drawn from each hard-wired section of the subdivided array. The clamping can be achieved by a single switch if the blocks are properly configured (and the switches in the arrangements are thermally operative), or if a diode matrix, as shown in Figure 49, is added to the array. On a local scale, the clamping can also be achieved by properly activating sets of switches within the more versatile reconfiguration arrangements. Finally, clamping can be achieved with individual switches placed with each hard-wired power block for the specific purpose of providing a clamp function. When this latter approach is taken, the clamping switch essentially acts as an on-off control for the individual blocks and greatly widens the range of uses for the clamp function.

Although disengaging the blocks of high voltage power into isolated power units may be an acceptable compromise to clamping in the initial outgassing phase or during the post-eclipse voltage stress conditions, it is interesting to pose certain system benefits of clamping locally. Collectively, the clamp switches can perform the following functions:

- A clamp for initial outgassing phase.
- A clamp for post-eclipse V_{oc} control.
- Dynamic protective clamp.
- On-off control of power blocks.
- A clamp to reduce peak power switched by reconfiguration switches.

The dual function of dynamic protective clamping and/or on-off control can be required because of some anomalous situation on the array, an interaction or shorting between loads, a load requirement for fast current or voltage reduction, or because of a special turn-on or shutdown sequence.

In general, if these functions are to be achieved by the reconfiguration switches rather than separate clamp switches, the total power being switched can easily become the major factor in determining the switch size and weight for either solid-state or mechanical devices. When individual clamp switches are provided, the reconfiguration switches need only to be capable of blocking high voltage and passing a maximum predetermined current and do not have to switch the power or change state under current flow conditions. This allows a system operation in which the interconnections of the

power blocks are modified the minimal number of times required to maintain proper load-power relationships for the major mission phases. For this concept, on-going dynamic control of the power reverts to the local clamp switches and regulation subsystem.

The clamp switches must be sized to switch the power of any given hard-wired block. For the largest block sizes considered in the present study, this means a maximum power switching capability of approximately 2.5 kv open circuit or 1.75 amperes short circuit. To utilize the clamp mode of control, the switch should be able to operate (assume and maintain either an open or closed state) at any time during the mission. This requirement can lead to complications for solid-state switches because of potential difficulties in activating these switches when exiting from eclipse without some measure of thermal control. In addition, the number of switching operations which the device must be able to perform influences the choice of the type of switch to reliably satisfy the requirements.

The use of solid-state switches to provide a clamping capability at the hard-wired block level during sunlit portions of the mission and a total array clamp in the form of the diode matrix clamp for initial outgassing and post-eclipse control presents an attractive system concept. This is discussed in more detail in Section 5 under Array Control.

5.4 BLOCKING DEVICES

Blocking devices, often employed with conventional low voltage solar arrays, take the form of blocking diodes. Their function is to eliminate loading of higher output sections of the array by sections which have a reduced output because of partial shadowing or a substantial failure due to shorting of internal points to a bus. If blocking were not provided to perform the above functions, it is possible that the energy exchange between higher and lower output portions of the array could lead to a catastrophic failure, electrically and/or mechanically, due to excessive thermal dissipation in the area where cells experience the inrush of current.

To a degree, the blocking requirements of the high voltage solar array include those of the conventional low voltage array. The major concerns, however, are those blocking requirements created either by the proposed methods of regulation and protective clamping or the type of loads that are to be powered by the array. As a result, the blocking devices required for the high voltage array have as their principle task the protection of electronics (switches). In performing this task, they also provide protection to the associated solar cells.

The configuration of the solar cell array for high voltage has carefully considered the requirements for elimination of possible shorts in the power source (solar cell power without electronics). Adequate spacing factors have been used and the array models have been configured without buses on the backside of the panel.

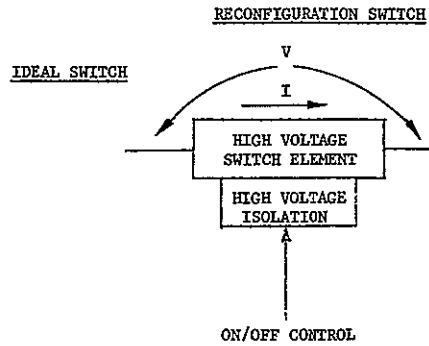
The blocking protection for the regulation and clamp switches used at the hard-wired block level is needed to assure operation within the power or voltage ratings of these switching devices. It is impractical from the standpoint of system performance to use oversized components to handle all the contingencies that can occur without blocking. The function of the clamp switches and the regulation switches (assuming a shunt removal regulation technique) is to short solar cell power. Under ideal conditions, the current rating of these devices would not need to exceed the maximum short circuit current of the power controlled. If reverse current from another source of solar array power is forced through the cells controlled by the switches, these switches would be required to pass the additional current to maintain control. When the switches are solid-state devices which pull out of saturation if the current exceeds that which can be passed for the drive power provided, high thermal dissipation results, leading to device failure.

The interchange of current leading to the problems discussed above can occur in at least three identifiable situations if blocking is not provided. The magnitude of the problem is, of course, related to the difference between the current generating capability of the cells which act as the load and those which forced the current. The first situation occurs when subdivisions of array power are combined into the basic hard-wired power blocks. This requires diodes internal to the block if the block is to be controllable and if it is composed of parallel sections. The second situation occurs when hard-wired blocks (not necessarily identical) are configured to power a given load by the reconfiguration switches. The third situation, potentially the worst, would occur when power configured to supply individual loads is shorted together, either by shorts between the load buses or shorts within a load requiring more than one source of power.

The requirements of the blocking devices can be satisfied by blocking diodes or reconfiguration switches which inherently have back blocking capabilities, even when in a control state allowing forward conduction (e.g., a device similar to a silicon-controlled rectifier). Because of the speed with which the back blocking action must be provided, achieving blocking by opening a mechanical switch would be unacceptable because of its long response times. This observation essentially establishes the criterion that mechanical reconfiguration switches should be used only in conjunction with blocking diodes or in reconfiguration arrangements having power steering diodes (see Figure 48) which accomplish blocking at the hard-wired block level.

5.5 RECONFIGURATION SWITCHES

Previous emphasis has been placed on the functional aspects of reconfiguring and controlling the solar array power. This section will concentrate on the reconfiguration switches required for mechanization. For the most part, this discussion is also applicable to high voltage switches which could be used to clamp the array as well as to those switches whose function, in certain switching arrangements, is solely to connect the configured power to the load (e.g., see Figure 48).



<u>Electrical Characteristics</u>	<u>Comments</u>
<u>Switch Element</u>	
Blocking Voltage, V:	≥ 16 KV, Bidirectional
Current, I:	to 1.75A (beginning of life, orbit raising mission)
<u>ON</u> Voltage Drop:	Low; affects reconfiguration efficiency and thermal radiation area.
<u>OFF</u> Leakage Current:	Low; affects thermal radiation area.
Power Switching Capability:	Full $I \times V$ desirable, but not essential
<u>Control Characteristics</u>	
Control Isolation:	≥ 16 KV
Control Mode:	Both ON and OFF with low level signal. (Pulsed or continuous signal acceptable)
Response:	Not critical; primarily a device problem of peak power dissipation.

Figure 50. Summary Electrical Specifications for an Ideal Reconfiguration Switch

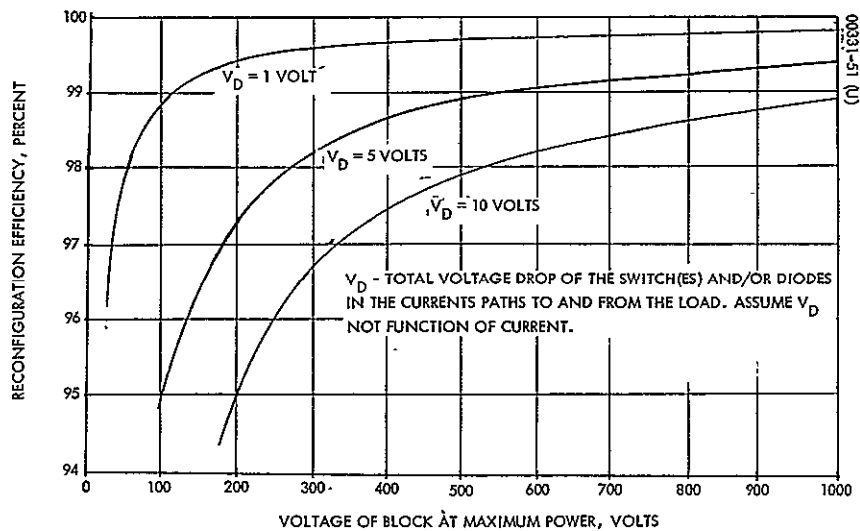


Figure 51. Effect of Switch and/or Diode Voltage Drops on Reconfiguration Efficiency as a Function of Block Voltage Sizing

The material concerning electronics placed on the panel, given in the regulation section, is applicable to the present discussion.

5.5.1 Electrical Characteristics

The electrical characteristics of desirable reconfiguration switches are related to the particular switching arrangement chosen for reconfiguration. For switching arrangements which have a high degree of flexibility for routing and recombining power, the current which the switch must carry becomes the major electrical variable. The required blocking voltage ratings, the preferred control characteristics, and the undesirability of high forward voltage drops remain essentially invariant. Considering reliability and array utility, it is desirable to configure arrays so that the distribution of the current carried by the individual switches is reasonably uniform.

The above considerations, together with the voltage and current requirements specified as study guidelines, have led to the summary specification of an ideal switch, shown in Figure 50. Certain of the characteristics are specified in terms of their effect on system performance or mode of operation. In general, the listed nonnumerical valued characteristics can be traded to achieve the listed numerical values.

Acceptable alternatives to the specified devices (assuming the numerical valued characteristics are achieved) are gate-controlled switches (GCS), silicon-controlled rectifiers (SCR), transistors, high voltage vacuum switches (relays) and switches made of multi-elements, termed composite switches. The closest analog to the ideal device, in terms of present solid-state technology, would be a photon-coupled thyristor operated in its linear region with the requirement that the device's holding current would exceed the maximum current to be passed under all anticipated environmental conditions.

The power transfer efficiency of the reconfiguration arrangement is directly dependent on the forward voltage drop of the reconfiguration switches and the blocking or power steering diodes used to mechanize the arrangement. Alternately, given that a particular efficiency must be achieved, the relationship between switching (and diode) voltage drops and the voltage magnitude of the power blocks can be developed. Figure 51 graphically presents general relationships between the reconfiguration efficiency, the voltage drops and the voltage of the power blocks. The curves were generated for the pre-assigned array (Figure 47) with identical voltage blocks; however, the trends indicated hold for all reconfiguration arrangements. The curves show a rapid drop off in efficiency for lower voltage blocks. Higher voltage blocks and current subdivision are usually preferred for load power matching.

The following three subsections discuss three classes of candidates for satisfying the switching requirements.

5.5.2 Mechanical Switches

Numerous classifications of mechanical switches exist. The two types which appear to present the most promise for use with the high voltage solar array are the ceramic enclosed vacuum relay and the vacuum dry reed switch relay. Of these two, the ceramic enclosed relay with latching capability is the most applicable and should lead to the minimum system weight penalty.

The ceramic enclosed high voltage vacuum relay represents the state of the art in high voltage relay design. It can withstand higher temperatures during degassing than its glass enclosed counterpart; hence, in general, a cleaner internal construction is achieved which enables the contacts to withstand higher voltages without breakdown. The devices presently being manufactured do not have mechanical configurations which lend themselves to placement on the panel; however, they could be incorporated rather easily into the deployment structure and located very close to the inboard edge of the panel. Special designs to achieve shapes which could be placed on the panel and deployed from indentations in the support structure are also possible.

It has been suggested that the relay should utilize the hard vacuum of space by removing the seal or portions of the enclosure from the relays. This suggestion appears to offer no real advantage and leads to many disadvantages. The present designs use the vacuum enclosure as the support structure for the stationary contacts and to maintain alignment of the mechanism. Even specialized designs would probably follow this same design approach. The portion of the enclosure that could be removed while still maintaining mechanical integrity would contribute little to reductions in weight or size.

The handling of unsealed relays on the ground for individual and system tests would be extremely difficult. It would be necessary to contain the unsealed relays within a controlled area, preferably a vacuum, to minimize or prevent contamination of the internal construction. Contamination of the contacts would result in degraded contact operation. The working voltage rating of the relay could be greatly reduced in space due to gases evolved from any contaminants. There appears to be no practical way in which unsealed relays could be adequately protected during the course of manufacturing, shipping, and installation.

Means for opening or removing the seal after launch, at some point in the mission, seem impractical. Even if there were a method of removing the seal in orbit, the local plasma would degrade the contact voltage rating. The contact gap, which is only several thousands of an inch, would be exposed to the plasma. The insulation resistance and breakdown voltage for the plasma would have to be equal to or better than that of the seal relay to justify the removal. The evidence against the in-space removal of the enclosure or the use of an unsealed relay clearly points to the use of enclosed relays.

The power which the switch must interrupt and the contact current rating have a strong impact on the weight of the switch. In general, they have a greater weight impact than the voltage rating of the contacts or the high voltage isolation between the contacts and the armature mechanism; hence, array control modes which do not require the interrupt of large amounts of power could lead to a weight reduction for specially designed relays. The weight saving would occur principally because of the reduced mass of the contacts and a smaller actuating mechanism.

Figure 52 presents in graphical form a survey of weight versus voltage rating capabilities for presently available ceramic enclosed high voltage vacuum relays. The contact arrangements for these relays are, in general, single pole-double throw. Curves are presented for both rated operating and peak test voltages. An additional curve represents estimates of nominal operating voltages that could be achieved by devices designed especially for high voltage solar array applications. The current capability of most of the relays used to generate the curves exceeds the output of the array in a 1000 volt configuration. It appears that relays satisfying the high voltage requirements (hold-off and control isolation) of an array switch would weight between 57 grams (2 ounces) and 85 grams (3 ounces).

The mechanical switch is not the ideal switch. Its basic shortcomings are a lack of inherent back blocking capability when on, a limited number of operations with reasonable reliability, and mechanical shapes and mounting methods that restrict its placement on the panel. One further problem which was considered in this study, but not completely resolved, is the effect of long-term exposure of the armature and the diaphragm seal to the hard vacuum of space. If these devices are chosen for use, experiments must be performed to evaluate the possibility of cold welding of the actuating mechanism.

5.5.3 Single Element Solid-State Devices

An investigation of solid-state devices capable of satisfying the reconfiguration switching requirements was undertaken. This included a review of the devices presently available, consultation with a number of device manufacturers, and certain basic calculations related to the blocking capabilities of multijunction solid-state devices.

Presently, devices are available which, except for blocking voltage and control isolation, approach the desired switch characteristics. From the standpoint of device feasibility, the blocking voltage rating is most important. The characteristic of blocking in both forward and reverse directions requires at least a two-junction device. Transistor switches were considered in the preliminary stages of the study, but they cannot be made in versions which stand off high voltage and block equally well in either direction. For this reason, the investigation concentrated on members of the thyristor family, of which the silicon-controlled rectifier (SCR) is the best known example. The regenerative characteristic of this device is particularly attractive because of the low average drive power required.

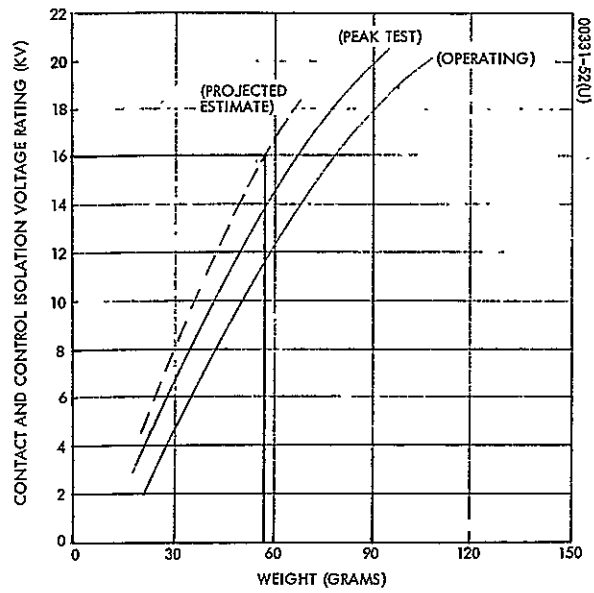


Figure 52. Achievable Voltage Ratings of Vacuum Enclosed Relays as a Function of Device Weight

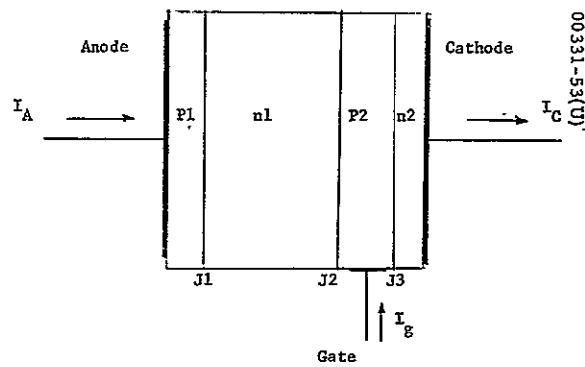


Figure 53. Structure of pnpn Device

Applicable extensions of the SCR are the light-activated switch (LAS) and the gate-controlled switch (GCS or GTO). The LAS is essentially a photon-coupled SCR, while the GCS is turned on and turned off via gate control pulses. It is desirable, but not essential, to be able to switch to the blocking state while carrying current. If it is impossible to develop such a high voltage switch, the hard-wired power blocks can be clamped to interrupt the current flow and allow the devices to revert to the blocking state before reapplying power.

Survey of Manufacture

Several manufacturers of SCR and related devices were consulted to obtain their opinion as to whether a 16 kv, 1.5 ampere SCR type device could be developed. Their comments on such a device were also invited. The results of the survey could best be described as inconclusive with regard to ultimate feasibility.

In general, most American manufacturers surveyed voiced considerable pessimism, since there is no SCR device produced in the United States with a blocking voltage rating greater than 3000 volts. In the last few years, the most impressive developments in high voltage SCRs have occurred in Japan. Representatives for a Japanese manufacturer of SCRs rated at 10 kv and 400 amperes indicated that a 16 kv device represents too large a step in technology to project feasibility and acceptable operating and control characteristics. Collective comments concerning the development of a gate-controlled switch were even more inconclusive. There was, however, reasonable agreement that extensions to a light activated device should offer no major problems if the technology could be developed to produce the basic 16 kv SCR type switch.

Device Design Considerations

Concurrent with the industrial survey, certain basic design areas for a conceptual 16 kv silicon solid-state device were investigated. The primary areas of consideration were volume (bulk) breakdown and surface breakdown of pnpn devices.

A typical pnpn structure of an SCR or GSC is shown in Figure 53. Breakdown of the blocking ability of the pnpn device results from either volume breakdown or surface breakdown. It is convenient to consider the two breakdown modes separately.

Volume Breakdown. As the device potential is raised, breakdown of the blocking capability of the bulk material of the pnpn device, and thus of one of its junctions, can be due to an avalanche process or to space charge layer spreading and punch-through. In the avalanche process, carriers accelerated in the electric field at a junction collide with the lattice and produce more carriers which are themselves accelerated in the field. These new carriers and the original ones are again accelerated by the field to produce new carriers and the process continues with further carrier multiplication.

Breakdown can also occur when the space charge layer spreads from one junction; e. g., from J1 for the reverse bias state, to an adjacent junction; i. e., to J2 for the present example. Such an event is termed punch-through. When it occurs, a space charge limited current flows, resulting in breakdown of the blocking characteristic.

In volume breakdown, the desired blocking voltage rating determines the required impurity density of the parent material and the width of the base region, nl. Consideration of the avalanche process and the required blocking voltage leads to a specification of the minimum impurity density allowable in the parent material. For asymmetrical junctions (ones in which the impurity densities are different on each side of the junction), the side with the smallest impurity density goes into avalanche first. In the pnpn device, region nl, which is the parent material (and has the lowest impurity density) is adjacent to junction J2, which blocks forward voltage and J1 which blocks reverse voltage. Therefore, the avalanche breakdown occurs in nl. For high voltage breakdown, the impurity density N_I for which avalanche breakdown occurs at voltage V_A , can be found by simultaneous solution (Reference 3) of:

$$V_A = \frac{b/E_m}{\frac{2a}{b} (1 - 2 \frac{E_m}{b})} \quad \text{and} \quad V_A = \frac{\epsilon E_m^2}{2q N_I}$$

where q is the electronic charge, ϵ is the permittivity, E_m is the maximum electric field at breakdown, and a and b are constants related to the ionization rates of holes and electrons. Using $V_A = 17000$ volts, $a = 1.6 \times 10^6$ per centimeter and $b = 1.65 \times 10^6$ volt/cm, N_I is found to be 5×10^{12} per square centimeter. There is no difficulty in achieving this impurity density.

Consideration of space charge layer spreading and punch-through leads to a specification of the width W of the nl base layer. For asymmetrical junctions, the space charge layer spreading takes place primarily in the region with a low impurity density, region nl. The width of the nl base layer must be made large enough to prevent the space charge layer from spreading across nl (from J2 to J1 for forward voltages, or from J1 to J2 for reverse voltages). The width W for which the punch-through voltage is V_{PT} can be found by solving the equation (Reference 4)

$$V_{PT} = \frac{q N_I W^2}{2}$$

for W . Assuming $V_{PT} = 17000$ volts and the impurity density specified by the avalanche process gives the value 0.21 cm for W .

Surface Breakdown. Breakdown in many high voltage pnpn devices is a surface phenomena rather than a bulk phenomena, i. e., the surface breaks down at a lower field than the bulk. This breakdown mechanism should present the major problem in extending present devices to the 16 kv level. The breakdown occurs because the carriers at the surface are less strongly bound than in the volume. Several methods can be used to reduce the field at the surface of the device, limiting the tendency to breakdown. A quad ring of higher resistivity semiconductor around the periphery of the blocking junction can be used to lower the field at the surface. Another technique is the use of high dielectric constant materials in contact with the surface to spread the field over a wider distance. Currently, the most successful technique is to properly contour the surface to reduce the surface field.

Beveling of the semiconductor surface at the p-n junctions is a practical way to lower the surface fields. Two types of beveling are possible. A positively beveled junction is defined as an asymmetric p-n junction having a linearly decreasing area from the more heavily doped side of the junction to the lightly doped side. The field decreases quite rapidly with bevel angle. A negatively beveled junction is defined as an asymmetric p-n junction that has linearly decreasing area from the lightly-doped side of the junction to the more heavily doped side. Positive beveling is much more effective than negative beveling in reducing the peak surface field. In fact, for some negative bevels the peak surface field is higher than for perpendicular surfaces.

Conventional bevel structures of pnpn devices use a positive bevel at junction J1 and a negative bevel at junction J2. However, since negative beveling is not very effective in reducing the surface field, the bevel angle must be less than 1 degree for blocking voltages higher than 3000 volts. The difficulty in achieving these small bevel angles explains, somewhat, why American devices are presently limited at the 3 kv level. This is very wasteful of semiconductor area. The loss of effective diameter of the silicon slice for the current carrying cathode will be more than 2 cm if the depth of the beveled region is 0.01 cm. The most effective contour (Reference 5) currently in use is called the double positive bevel and receives its name because both junction J1 and J2 now have the positive bevel. This concept has been used by the Japanese in the production of 7 kv and 10 kv SCR devices which have forward voltage drops between 1 and 2 volts when conducting 10 to 200 amperes.

Potential Design Problem Areas.

An important area of concern in the development of a 16 kv SCR is the power generated in the device in the blocking state. The blocking power is a rapidly increasing function of junction temperature (through dependence on blocking or leakage currents). If the power generated becomes greater than the capability of the heat sink to reject it, thermal runaway occurs, causing triggering to the on state if forward voltage is applied, or possible destruction of the device if reverse bias exists. Providing sufficient

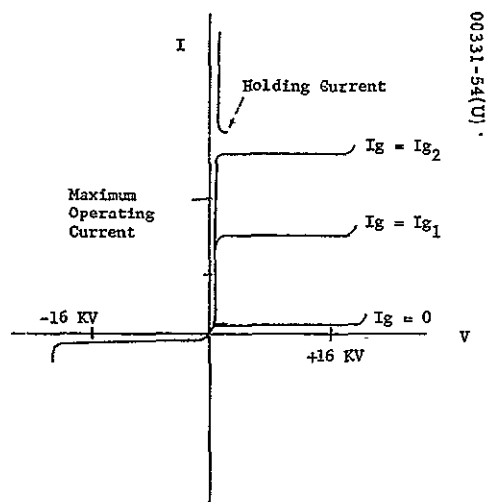


Figure 54. Desirable pnpn Device Characteristics

heat rejecting thermal radiation area to handle this dissipated power at high voltage may prove difficult, especially with the device placed directly on the panel. At present, this is projected as a possible problem area, assuming that device development is electrically and economically feasible.

Another potential design problem related to environment arises because of the temperature dependence of the avalanche process. The avalanche breakdown voltage of a junction decreases with decreasing temperature. Normal ratings on SCRs specify -40°C as a lower operating limit. The solar array, however, may see temperatures as low as -180°C during an eclipse. A quantitative description of the temperature dependence of the avalanche process at these low temperatures is required to determine whether the high voltage SCR can be used directly on the array and withstand post-eclipse voltage without thermal control during eclipse.

Several other ratings or characteristics of pnpn devices can become difficult to control when the device is designed for high blocking voltage capability. However, in many cases the performance can be partially or totally recovered through the use of different construction techniques. For example, the device turn-on time, di/dt capability, dv/dt capability, and on-state voltage drop are adversely affected by the requirement of a large voltage blocking capability. Improvement in the turn-on time and di/dt capability can be made through the use of various cathode-gate configurations such as the field initiated gate construction reported by Ohtsuka (Reference 5). The dv/dt capability can be increased through the use of a shorted emitter construction which shunts capacitive current around the emitter junction so that turn-on will not occur. On-state voltage drops can be reduced by using techniques to increase the minority carrier lifetimes. Such techniques may also be necessary to insure that the device will switch on and be tolerant to reasonable particulate radiation. A gated turn-off capability may be made possible by using an interdigitated gate-cathode assembly.

It has been mentioned that special techniques should be used to insure that the pnpn device will switch to and hold the forward conducting state. It may be advantageous, instead, to prevent its doing so. As mentioned, earlier, it is desirable to be able to turn the device off as well as on. In practice this has proven difficult to do with SCR or GTO structures. These structures typically have to be derated to provide the turn-off capability. However, the pnpn device would turn off with the removal of gate drive if it had the characteristics shown in Figure 54; i.e., if it operated in a linear mode. The device would probably also require less drive current I_g for the "on" state than an equivalent transistor because of the regenerative action in the pnpn devices. And, unlike the transistor, it could block equally well in forward and reverse directions. A further desirable advance to reduce the complexity of high voltage isolation for control would be an SCR with the characteristics shown in Figure 54; i.e., a LAS operated in the linear mode. The symbol I_g in this case would relate to values of irradiance of the driving photon source.

A reliable high voltage solid-state switch with turn-on and turn-off capabilities, inherent high voltage isolation for control, and with bidirectional blocking properties would lead to the ideal reconfiguration and power control system. Members of the thyristor family of switching devices appear to have the greatest potential of achieving the switching goals. Nothing from the investigation of this study precludes the development of such devices. In fact, because of the moderate power levels required for the high voltage array and the rapid advances posted by the Japanese the outlook technologically is optimistic.

5.5.4 Composite Switches

The solid-state devices that are presently available which can function as switches do not have voltage ratings which satisfy the requirements of a reconfiguration switch or a clamp switch. In the early portions of the study, the possibility of meeting the high voltage specification with composite switches composed of individual switch elements and fabricated using hybrid construction techniques was investigated in considerable detail.

The electrical configurations of the composite switches considered were basically series arrangements of high voltage transistors, silicon-controlled rectifiers, or gate-controlled switches. Consideration was also given to series-parallel arrangements to distribute power dissipation over large areas. Control techniques included direct drive and intermediate drive stages powered from small solar cell bias sections located with the switch. Both transformers and photon-coupled high voltage control isolation were considered. The results of the investigation were discouraging based upon projected performance for switch configurations using presently available devices. A clear need was seen for improved devices. The composite switch technique looks attractive for solid-state clamp switches used at the hard-wired block level. Series connected photon-coupled transistors are satisfactory in this function because bi-directional blocking is not required.

The composite switch approach is one way of achieving a high voltage solid-state switch without requiring a single element to withstand the total blocking voltage. It offers economic and technical alternatives to the development of a solid-state switching device. An improvement in the number of series elements required and the relative power handling efficiency of the switch is dependent on the ability to push technology to achieve higher voltage ratings with lower voltage drops and reduced control power. Such advances in technology can partially offset the major problems associated with the composite switch, higher power dissipation because of series multiple junctions, required static and dynamic voltage stress equalization, and increased drive power and/or drive circuit complexity.

Because of the reasons discussed in the previous section, it is concluded that members of the thyristor family represent the most attractive single elements from which to configure composite switches used for reconfiguration. Effort expended on developing a single element high voltage device with satisfactory control characteristics and the ability to withstand the mission environmental conditions can be recovered, even if the maximum ratings are not achieved, by employing the devices in composite arrangements.

5.6 ARRAY CONTROL

In this subsection the operational logic for controlling the array power will be discussed. The particular control functions of interest are: reconfiguration, dynamic protection by clamping at the hard-wired power block level, and total array clamping. When these functions are integrated into a system, there can be overlapping in the functions performed by individual devices and by the logic involved in controlling the devices. In addition, since there are reconfiguration switching arrangements which can inherently provide all of the above functions, the control of the array power (less the fine control of regulation) can fall under the broad terminology of reconfiguration.

The actual hardware design of the on-board electronic is a low voltage logic design problem. When high voltage isolation is provided for the switch control signals and for sensing, and when switches are available which satisfy the requirement of the high voltage array, the detailed design of the low voltage logic circuitry will follow conventional methods. Therefore, array control is discussed in terms of switching operations.

Preferred modes of control for the high voltage solar array are determined by the switching devices chosen (or available) for mechanization, by mission environmental factors, and by the load requirements. The thermal conditions in eclipse orbits are a major factor since they can preclude the satisfactory operation of solid-state switches without artificial thermal control at exit from eclipse. When mechanical switches are used to provide a clamp for exiting eclipse, the number of eclipse periods determines operational reliability.

Because of the dependence of the modes of control on the devices used, the operational logic of control for two desirable approaches to system mechanization will be presented. One system is assumed to use mechanical switches for recombining and routing the hard-wired power blocks. The other is assumed to be configured with high voltage solid-state switches. In addition, it is assumed that these switches (mechanical and solid-state) will not interrupt power; hence, they are designed to block voltage and conduct current. This would, for example, allow the use of high voltage SCRs as the solid-state device. Lighter weight devices and improved reliability would also result.

For both systems, a solid-state clamp switch is incorporated with each hard-wired block. All solid-state switches (including the regulation switches) are assumed to be inoperative until thermal equilibrium has been reached following eclipse. Also, each system is assumed to have a total array clamp for protection during the initial outgassing phase of the mission and for overvoltage protection upon exiting eclipse.

As previously mentioned, certain routing and combining arrangements have the capability of self-clamping. When mechanical switches are used in such arrangements, total clamping could be achieved at any time in

the mission with little regard to the thermal environment. However, for the proposed mission, many switches would have to switch under current flow conditions, and the number of operations would adversely affect projected switching reliability unless switch redundancy was provided. This mode of operation is possible but it is considered undesirable. When the assumptions concerning the switches to be used in the two systems are considered, the preferred approach is the diode matrix clamp previously shown in Figure 49. Since this system has a single switch function, the required switching reliability could easily be achieved with simple switch redundancy.

Either of the two system mechanizations are applicable to the specific and universal array models.

5.6.1 A System with Mechanical Reconfiguration Switches

The basic assumptions for this system are repeated:

- 1) Reconfiguration switches are mechanical and are not required to switch under current flow conditions.
- 2) A solid-state clamp switch (for on-off control) is placed with each hard-wired power block.
- 3) All solid-state switches (individual clamps and regulation) are not operated until the array is at thermal equilibrium.
- 4) A total array clamp is employed.

Starting from predeployment, the approach to the control of the array through the use of individual switch groupings is now discussed.

- 1) Initial Outgassing Phase – Prior to array deployment, the state of the total array clamp is set. Following deployment and the initial outgassing phase, the system is ready for normal operation.
- 2) Eclipse Exit Control – The total array clamp (for each eclipse orbit) is maintained until the thermal operating temperature of the solid-state devices has been reached. This typically should occur concurrently with the thermal equilibrium of the array.
- 3) Start Up – The solid-state clamp switches are activated. The mechanical reconfiguration switches should be in their proper states to combine and route the hard-wired power blocks. If a new configuration is desired, different from that used in the previous sunlit period, the states of the reconfiguration switches are reset at this time. With the array under solid-state clamp control, the total array clamp is removed. The solid-state clamp switches are deactivated and power is applied to the loads which are assumed to be in a state of readiness to accept the power. For each load, because of the controllability of the

clamp switches, the power from the hard-wired blocks can be applied sequentially or simultaneously. If sufficient control range is provided in the controllable power blocks, a combination of clamp and regulation switches can provide a smooth ramp of voltage at turn-on. Because of the inherent capacitance of the array and the effective capacitance between the space plasma and the array, the rate of rise of voltage is slowed. This latter phenomenon, which is dependent on plasma density, is briefly discussed in Appendix F and should create no basic problem in the system's operation. Loads requiring faster applications of power than those possible with the clamped mode of turn-on can employ a load switch. In this case, the array output for the given load would be adjusted by the regulation system to a nominal value commensurate with the expected load current and with the state of the solar cell source. The power would then be applied. The regulation subsystem would quickly compensate for minor deviations.

- 4) Dynamic Protection – During system operation, intermittent abnormalities can be expected to occur in the loads. Although the solar array has a current limiting characteristic, the block current sizing, particularly in the early portions of the missions, may exceed that which can be tolerated by the load. In these situations, the solid-state clamp switches can be used individually as extensions of the regulation system and quickly produce a gross modification of the load power and I-V characteristics. In general, the combination of regulation and solid-state clamp switches can provide corrections continuously from a minor change in the output to total crowbar action. The required sequence of events can be tailored to meet the need of any high voltage load through specific design features in the low level logic that controls the state of the switches.
- 5) Shut Down – The sequence of events for shut down can vary slightly depending upon the reason for initiation: a total malfunction of a load, a desired reconfiguration of power, or vehicle approach to eclipse. In any case, the solid-state clamp switch will be used with the power participating in the shut down. For the case of the vehicle approaching eclipse, the state of total array clamp would be set in preparation for providing eclipse exit control.
- 6) Reconfiguration – The states of the mechanical reconfiguration switches can be changed at any period during the orbit by an on-board programmer whose state has been established by ground command. Verification that satisfactory reconfiguration has taken place can be a part of the start up sequence following reconfiguration if the state of the reconfiguration switches was changed during eclipse. Load sensors in combination with the solid-state clamp switches would allow reconfiguration to be affirmed for each hard-wired block individually and prior to

applying full power to the loads. If the state of the reconfiguration switches is changed during sunlight conditions, the power blocks involved would be clamped, the reconfiguration switches activated, and the verification check-out established above employed.

5.6.2 A System with Solid-State Reconfiguration Switches

Both the mechanical switch system and the solid-state switch system have similar modes of operation. This results from the requirements for switch turnoff during noncurrent flow conditions. In spite of this similarity, details of the system operation will be listed, as in the previous section.

The basic assumptions for this system are:

- 1) Reconfiguration switches are solid-state and are not required to switch under current flow conditions. This would allow the use of SCR type devices.
- 2) A solid-state clamp switch (for on-off control) is placed with each hard-wired power block.
- 3) All solid-state switches are not operated until the array is at thermal equilibrium.
- 4) A total array clamp is employed.

The procedures for using the switches to meet the functional control requirements are presented below.

- 1) Initial Outgassing Phase — Prior to array deployment, the state of total array clamp is set. Following deployment and the initial outgassing phase, the system is ready for normal operation.
- 2) Eclipse Exit Control — The total array clamp (for each eclipse orbit) is maintained until an acceptable operating temperature is reached.
- 3) Start Up — The solid-state clamp switches are activated. Following activation, drive signals are initiated to those solid-state reconfiguration switches which are required to be on to establish the desired configuration of hard-wired blocks. With the array under solid-state clamp control, the total array clamp is removed. The solid-state clamp switches are deactivated and power is applied to the load. The power may be applied sequentially or simultaneously. The combinations of clamp and regulation switches can be coordinated by control logic to give a wide range of turn on characteristics. Loads requiring the instantaneous application of power can use a separate load switch.

- 4) Dynamic Protection— The requirements for dynamic protection can be met in the way already discussed for the mechanical system.
- 5) Shut Down— The same procedure as in the mechanical system would be employed.
- 6) Reconfiguration— The state of the solid-state reconfiguration switches would have to be re-established by the control drive signals for each period of operation. However, the on-board logic providing the drive would hold its state unless reconfiguration was requested by ground command. In this sense, the solid-state system is analogous to the mechanical system; hence, verification that the reconfiguration switch logic has received the proper commands would proceed like the mechanical system. Because of the speed with which the verification could be undertaken with an on-board computer in combination with the solid-state clamp mode of control, it would seem advisable to include such verification as a normal step in the start-up sequence.

5.7 SUMMARY CONCLUSIONS

Reconfiguration switching arrangements using both mechanical and solid-state switches have been considered. No single element solid-state device presently available can satisfy the high voltage requirements; however, SCRs or other members of the thyristor family of devices have most of the characteristics desired. From estimates of projected device weights for mechanical high voltage vacuum enclosed latching relays and for single element solid-state switches (including thermal radiating area and weight associated with power dissipation), it is concluded that systems requiring few reconfiguration operations and mechanized with either switch type would be comparable in weight. In certain situations, a solid-state device could be preferred. A choice of the solid-state device would be based on the requirement for a large number of switching operations, inherent fast bidirectional blocking capabilities, and more compatible mechanical dimensions for placement on the array. However, in light of the array control modes discussed in the text, the use of mechanical latching reconfiguration switches is not undesirable.

Various array clamping procedures were considered. The combination of a total array clamp and an on-off clamp switch placed with each hard-wired block leads to a very simple array control procedure. A solid-state clamp switch (requiring an intermediate voltage rating ≤ 2.5 kv) at the block level would provide fast control of the power blocks and would, if operated in combination with the regulation subsystem, allow full range control of each output during sunlit portions of the missions. All dynamic protection, array start-up, and diagnostic interrogation switching would be performed by these devices. The individual clamp switches would allow

reconfiguration under sunlit conditions with no current flow in the reconfiguration switches, would reduce their size, and would simplify device design.

From the standpoint of reconfiguration and power control, the high voltage solar array is conceptually a simple approach for providing conditioned high voltage power to multiple loads. Aside from the control logic, very few additional components are required; basically, high voltage and intermediate voltage (clamp) switches with high voltage control isolation and sensors with high voltage isolation. When the switches are available and the high voltage isolation is provided, the hardware design of the control logic which activates the switches based on sensed parameters and desired system operation, should be straightforward. No major difficulty is expected in mechanizing the reconfiguration and power control concepts presented.

Certain key questions have been isolated. The feasibility of the single element solid-state reconfiguration switches should be conclusively established in terms of both technical and economic factors. Special vacuum relay designs which could reduce weight and increase reliability in the vacuum environment should be studied. The results of the dual investigations would indicate the expected return on additional development effort and the direction it should take.

6. PERFORMANCE ESTIMATES

6.1 PERFORMANCE INCREMENT CALCULATIONS - ARRAY EFFICIENCY

Performance increments are defined as weight and area changes per unit power for specific high voltage design actions. Increments are developed through comparison of the configured array models with a base conventional low voltage array specified in the study contract.

Two array models have been employed, a universal model and a specific model. The final array design is expected to lie between the two performance boundaries established by the models.

In addition to the development of performance increments for both models, the impact of conductive coatings on performance is presented. Conductive coatings are proposed as an alternative design action in the study. These coatings would allow substrate and coverslide thicknesses comparable to the base conventional array to be used. Without coatings, greater thicknesses are required to withstand charge buildup in the plasma environment. Increments are shown for both models with and without conductive coatings.

The tabular listings represent beginning-of-life performance. End-of-life performance is added in summary form by bar-graph presentation. The effects of environmental degradation for a 5-year orbit raising mission are shown for the conventional array as well as the high voltage models.

The assumptions employed in computation of performance increments are presented below.

6.2 TABULAR CATEGORIES (TABLE 4) - BEGINNING OF LIFE

6.2.1 Panel Categories

Substrate

Thickness

Conventional array - 0.0025 cm (1 mil)

High voltage arrays - 0.013 cm (5 mils)

High voltage arrays with conductive coatings - 0.0025 cm (1 mil)

TABLE 4. SOLAR ARRAY EFFICIENCY - TABULATED

	Conventional Array		Specific High Voltage Array with Conductive Coating		Universal High Voltage Array with Conductive Coating		Specific High Voltage Array		Universal High Voltage Array	
	Area	Weight	Area	Weight	Area	Weight	Area	Weight	Area	Weight
Panel										
Substrate			0%	0.4%	0%	0.4%	0%	12.5%	0%	12.5%
Coverslide			0	0.3	0	0.3	0	10.0	0	10.0
Borders			1.1	0.1	1.8	0.1	1.1	0.2	1.8	0.3
Bus Area			0	0	10.2	0.3	0	0	10.2	1.6
Bridging			0	0	0	0	0	0	0	0
Diodes			0	0	3.6	2.0	0	0	3.6	2.5
Bus Weight			0	-3.7	0	-2.2	0	-3.7	0	-2.2
Insulation			0	0	0	-1.3	0	0	0	-1.3
Total Percent Δ			1.1	-2.9	15.6	-0.4	1.1	19.0	15.6	23.4
Efficiency	107 w/m ²	14.6 kg/kw	106 w/m ²	14.1 kg/kw	94.5 w/m ²	14.5 kg/kw	106 w/m ²	17.3 kg/kw	94.5 w/m ²	17.9 kg/kw
Regulation										
Leads			0.5%	0.1%	0.6%	0.3%	0.5%	0.1%	0.6%	0.3%
Logic			0	0.1	0.2	1.2	0	0.1	0.2	1.2
Switches			0.2	1.2	0.2	1.2	0.2	1.2	0.2	1.2
Cells			0.2	0.3	0.4	0.4	0.2	0.3	0.4	0.5
Subtotal			0.9	1.7	1.4	3.2	0.9	1.7	1.4	3.2
Configuring										
Switches			0.1%	1.6%	0.3%	6.9%	0.1%	1.6%	0.3%	6.9%
Clamps			0	0.5	0.1	1.2	0	0.5	0.1	1.2
Diodes			0.1	0.8	0.1	1.2	0.1	0.8	0.1	1.2
Subtotal			0.2	2.9	0.5	9.3	0.2	2.9	0.5	9.3
Total Percent Δ			2.2	1.7	17.5	12.1	2.2	25.6	17.5	35.9
Efficiency (cumulative total)	107 w/m ²	14.6 kg/kw	105 w/m ²	14.8 kg/kw	91.5 w/m ²	16.3 kg/kw	105 w/m ²	18.3 kg/kw	91.5 w/m ²	19.8 kg/kw
Conventional Power Conditioning		24.9%								
Configuring		8.1								
Total Percent Δ		33.0								
Efficiency (cumulative total)	107 w/m ²	19.4 kg/kw	105 w/m ²	14.8 kg/kw	91.5 w/m ²	16.3 kg/kw	105 w/m ²	18.3 kg/kw	91.5 w/m ²	19.8 kg/kw
Overdesign	8.7%	8.7%	6.0%	6.0%	11.2%	11.2%	1.0%	1.0%	6.2%	6.2%
TOTAL	99 w/m ²	20.6 kg/kw	99 w/m ²	15.6 kg/kw	82 w/m ²	18.1 kg/kw	104 w/m ²	18.5 kg/kw	86 w/m ²	20.9 kg/kw
Efficiency	(9.2 w/ft ²)	(45.5 lb/kw)	(9.2 w/ft ²)	(34.5 lb/kw)	(7.6 w/ft ²)	(39.9 lb/kw)	(9.7 w/ft ²)	(40.7 lb/kw)	(8.0 w/ft ²)	(46.2 lb/kw)

Coverslide

Thickness

Conventional array—0.008 cm (3 mils)

High voltage arrays—0.015 cm (6 mils)

High voltage arrays with conductive coatings—0.008 cm (3 mils)

Solar Cell

It is emphasized that a 0.02 cm (8 mil) solar cell was assumed for both the high voltage and conventional arrays in increment calculations. This was done, in spite of the use of 0.015 cm (6 mil) cells on the proposed high voltage arrays, to avoid unfair advantage to the high voltage array. The baseline conventional array employs 0.02 cm (8 mil) cells. This assumption increases the weight of a single cell with coverslide by approximately 13 percent.

Borders

Spacing

Conventional array—0.13 cm

High voltage array—1.5 cm

The weight difference with conductive coatings results from decreased thickness of the substrate for the border area.

Bus Area

Conventional array—0 (buses are on backside)

High voltage array—1.8 cm/bus

The specific model has no buses. The weight difference with conductive coating for the universal model results from decreased thickness of the substrate under the buses.

Bridging

Bridging refers to insulation of bus crossover of regulation leads to the blocks. The effect on performance increments is negligible.

Diodes

The method of incorporation of bypass diodes on the specific array imposes no penalty. The copper strips for diode mounting employed with the universal array cause weight and area loss. The weight difference with conductive coating for the universal model results from decreased thickness of the substrate under the copper diode mounting strips.

Bus Weight

The specific array is a busless design. Buses on the universal array are sized in cross sectional area to give a power drop equivalent to the conventional array.

Comparison was made to the conventional array as presented. No attempt was made to increase the bus size of the conventional array, as would probably be necessary, to carry total power equivalent to the high voltage array.

Insulation

The insulation is bus insulation. The specific array has no buses. Buses on the universal array are unencapsulated.

6.2.2 Regulation and Configuring Categories

The power conditioning which is included with the universal and specific array models, is presented in separate functional categories to more clearly identify the origin of the weight and area increments incurred. The weights and panel areas attributed to power conditioning components for regulation and reconfiguration must be recognized as preliminary estimates. The accuracy of the estimates for the regulation components, particularly the intermediate logic and regulation switches, is dependent upon achieving satisfactory packaging for the anticipated environment. The weight of the reconfiguration switches is close to that now achievable with high voltage vacuum latching relays (see Figure 52). This weight should represent a good estimate of the total system weight penalty that would exist if a device of the thyristor family were developed to satisfy the switch requirements and employed in the switching arrangement. It should be noted that the projected total system weight and area is quite insensitive to small inaccuracies in the estimates of power conditioning component weights and areas.

The assumptions used for each of the array models is now briefly outlined.

Universal Array

Regulation

- 1) All 500 volt subdivided power blocks are controllable 0 to maximum voltage, with 14 switches per block.
- 2) Intermediate logic is associated with each of the controllable 500 volt blocks. This logic contains the high voltage interface isolation.

- 3) Logic size and weight for blocks having 1, 2 or 3 cells in parallel are assumed identical. Drive power to each regulation switch assumed as 20 mw at end-of-life. Only intermediate voltage isolation (≤ 1 kv) is required between logic and switches.
- 4) Thermal radiating area of regulation switches based on 13 cm^2 (per side) per watt dissipated at beginning-of-life and a 1 volt switch drop when passing short circuit current.
- 5) Solar cell bias power sized to power intermediate logic and all regulation switches at end-of-life.

Reconfiguration

- 1) The 180 subdivided power blocks are combined into 45 hard-wired blocks.
- 2) A preassigned reconfiguration switching arrangement is employed (see Figure 47). Each of 45 hard-wired blocks can be switched (on the average) to two locations requiring 180 switches. The 90 locations require 90 continuity diodes.
- 3) A clamp switch is associated with each of the hard-wired blocks. The maximum short circuit of any hard-wired block at beginning-of-life is 1.75 amperes.
- 4) The following average weight and area values were assumed:

	<u>Weight, grams</u>	<u>Area, cm^2</u>
Reconfiguration switches	85	26
Clamp switches	57	26
Diode assemblies	28	13

These values should be equally applicable to either mechanical switches or a developed solid-state switch of the thyristor family. Each switch is assumed to contain the high voltage interface isolation.

Specific Array

Regulation

- 1) Seven of the 16 blocks are controllable over their full range, with 16 switches per block.
- 2) The regulation switches have a 1 volt drop at beginning-of-life when passing short circuit current. Drive power (100 mw per switch at end-of-life) is provided via intermediate logic which contains the high voltage interface control isolation.

- 3) The thermal radiating area of the regulation switches is based on 13 cm² (per side) per watt dissipated at beginning-of-life.

Reconfiguration

- 1) The reconfiguration switching arrangement is assumed to follow the simplified arrangement shown in Figure 48. The number of components and the estimated average values of weight and area of each is:

	<u>Weight, grams</u>	<u>Area, cm²</u>
27 reconfiguration and load connect switches	85	26
16 clamp switches	57	26
32 diode assemblies	28	26

Each of the above switches is assumed to contain the high voltage interface isolation.

6.2.3. Conventional Power Conditioning and Configuring Categories — Conventional Array

In order to provide a comparison between the conventional and high voltage solar array concepts, the estimated weight of power conditioning for a conventional system is given.

The weight increment listed under the category of conventional power conditioning includes the weight of power conversion from a low voltage bus and the required regulation circuitry. The conventional system is assumed to be constructed in modular form. The output of each module would be sized in voltage and power capability to correspond to the hard-wired power blocks of the high voltage array. Improved system reliability would be achieved by having partial standby submodules within each block. With this approach, the range of load regulation control and the requirements for reconfiguration switching should be similar to the high voltage array approach.

The system weight increment was assumed to be 3.6 kg/kw with partial sub-module redundancy. The penalty for configuring is assumed to be equal to the switch and diode increments associated with the universal high voltage array, 1.2 kg/kw. The power efficiency of the power conditioning is assumed to be 92 percent. The incremental penalty for this is listed separately under the category of overdesign.

6.2.4 Overdesign Category

The category of overdesign refers to the requirement for additional power on the panel to compensate for inefficiency. Inefficiency for the conventional array is related to required power conditioning for high voltage operation. In the case of the high voltage array, it relates to the efficiency of load matching, together with optical transmission loss in the use of conductive coatings. The choice of overdesign value for each array is discussed briefly below. It is assumed that the weight and area penalties are equivalent.

Conventional Array

The figure of 8.7 percent is based on Hughes hardware. It is applied to the conventional array kg/kw prior to the addition of regulation and configuration weights.

Specific Array—Conductive Coatings

Based on software development in this study, it is assumed that load matching capability is 99 percent. As a result, overdesign of 1 percent is required. An additional 5 percent loss is added for transmission loss due to the conductive coating.

Universal Array—Conductive Coatings

Computations indicate that the 180 block universal array has a load matching efficiency of 93.8 percent. As a result, overdesign of 6.2 percent is required. An additional 5 percent loss is added for transmission loss due to the conductive coating.

Specific Array

Comparable to the specific array with conductive coating. No coating is employed.

Universal Array

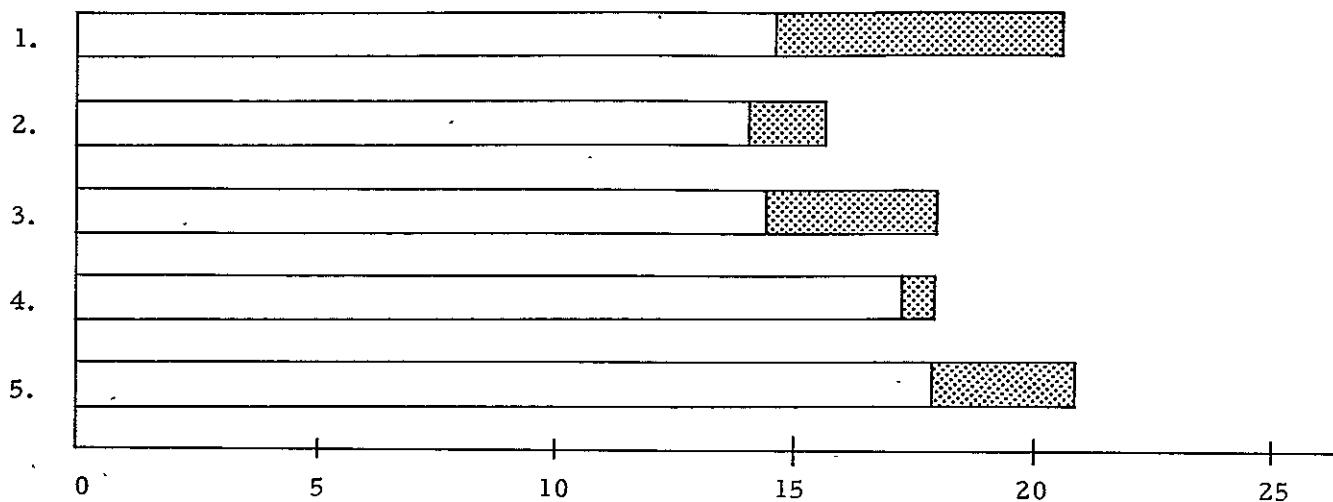
Comparable to the universal array with conductive coating. No coating is employed.

6.3 BAR GRAPH CATEGORIES (TABLE 5)—BEGINNING AND END OF LIFE

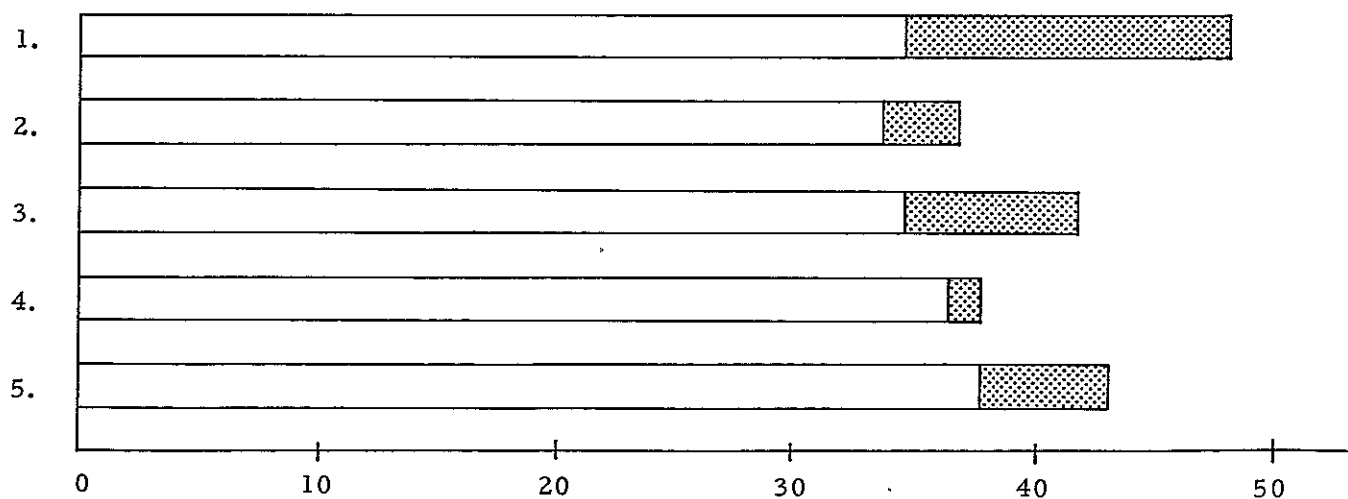
The summary bar graph presentation of end of life performance, for both the high voltage and conventional arrays, employs the conventional array cell thickness of 8 mils. The radiation environment in the 5-year orbit raising mission is the same for both arrays and was defined in Appendix A. Performance predictions for the high voltage array in the main body of this report were based on the proposed 0.015 cm (6 mil) solar cell.

TABLE 5. SOLAR ARRAY EFFICIENCY - BAR GRAPH

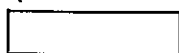
1. Conventional array
2. Specific high voltage array with conductive coatings
3. Universal high voltage array with conductive coatings
4. Specific high voltage array without conductive coatings
5. Universal high voltage array without conductive coatings



SPECIFIC WEIGHT, kg/kw, BEGINNING OF LIFE



SPECIFIC WEIGHT, kg/kw, END OF LIFE (ORBIT RAISING MISSION)



SOLAR PANEL ONLY



POWER CONDITIONING AND OVERDESIGN

Note should be made that the weight advantage of the array with conductive coatings tends to be lost at the end of life. This results because of the rather severe radiation environment during the proposed mission. The thinner coverslides resulting from the use of conductive coatings offer less protection from radiation damage.

RECOMMENDED FUTURE EFFORT

7.1 PROBLEM AREAS

During the course of this study, numerous problem areas have been identified. Most of these have been discussed in other sections of this report. The major anticipated problems with power conditioning implementation for the high voltage solar array relate to the development of reliable switching devices and electronic circuitry to perform the necessary functions of regulation, control and reconfiguration. In particular, the reconfiguration switches and the high voltage isolation for control and sensing are areas where failures could have a profound effect on total system operation. The thermal environment established by the eclipse orbits is of special concern to the packaging of electrical components placed on the array.

The problems involved in fabricating and testing high voltage arrays with integral power conditioning are discussed in Subsection 3.2. Early follow-on tests performed with small scale breadboards will be useful in establishing base-line preferential system testing procedures.

Most of the key high voltage problem areas concerned with high voltage panel design were defined in the first study (Reference 1). In general, the problem areas involve determination of material properties, under combined mission environments.

Because of concern for array performance in the present study, a very practical problem was isolated in the panel design and should be emphasized. A major performance increment penalty for high voltage design is the required thickness of the substrate and coverslides necessary to withstand charge buildup in the plasma environment. Methods for breaking this thickness barrier have been proposed. This item should be further considered in future studies.

7.2 FOLLOW-ON EFFORT

7.2.1 Power Conditioning Related

The effort in this area should principally involve device development and system concept evaluation using scaled model breadboards. Although

mechanical switch devices appear satisfactory for reconfiguration use, the feasibility of a solid-state switch with reverse blocking capability should be determined.

Analytical and Experimental High Voltage Switch Studies

The feasibility and economic aspects of developing an acceptable single element high voltage solid-state reconfiguration switch must be resolved. Concurrent with this investigation, a mechanical switch study should be undertaken to conclusively assess the weight and physical configuration of a device specifically developed for high voltage array use. The results of the dual investigation would indicate the expected return for additional development effort and the direction it should take.

Scale Model Breadboard

The concepts suggested in this study require verification and refinement. Breadboard testing is recommended. The development of these breadboards could proceed in phases from the initial concept evaluation phase to a final full environmental testing phase. The initial phase would involve construction of a low power panel using the high voltage panel design guidelines. This panel would be divided into a number of low power blocks (e.g., four 500-volt blocks, each with an output power level of 25 watts) allowing a range of output up to 2000 volts and 100 watts. All regulation, clamping and reconfiguration components would at first be off the panel. Presently available components in combination with the panel could be used to mechanize the control concepts. Full electrically evaluation could be undertaken.

As packaged components are developed, which are compatible with placement on the array, they would be incorporated. When the panel had a full complement of components, both environmental and electrical tests would be conducted.

Solid-State Control Switch

Development design studies for the regulation and clamp switches should be performed. Devices with integral high voltage photon-coupled isolation would be of particular interest.

Sensors

A development design study should be undertaken to develop a digital-to-analog sensor with high voltage isolation.

Electronic Packaging

Perform detail design studies of packaging techniques for electronics proposed for placement on the panel. The studies should specify and test fabrication procedures for on-panel switches, diodes and logic. This task should be coordinated with or be a part of, the component development studies.

7.2.2 Panel Related

As in the problem area, follow-on effort which would influence high voltage panel design has been developed in detail in the first study (Reference 1). The experimental work in material properties and the breadboard panel testing defined in that study are re-emphasized.

Certain items requiring special emphasis as a result of the present study are indicated below.

Soft-Reverse Characteristic Solar Cells

The ability to reliably produce cells with soft-reverse characteristics could eliminate the need for bypass diode protection from open failure.

High Voltage - Low Current, Multijunction Solar Cells

Development of the high voltage cells, described conceptually in the present study, would provide efficient coverage for low current loads.

Dielectric Sizing Principle

An experimental evaluation of the factor of 2, thickness sizing principle employed for array dielectrics is suggested. The weight penalty for the dielectric substrate and coverslide impels detailed consideration of the chosen thickness.

Conductive and Semiconductive Coatings

If the above thickness barrier for substrate and coverslide are confirmed by test, conductive coatings should be studied to break this barrier. The coverslide coating is of primary concern, requiring high transmission and a minimum of 1 micron thickness.

Backside Radiation Effects

Assess the equivalent thickness principle developed in this study. Work now in progress at Hughes and in the rest of the industry may be sufficient. Particular attention should be given to varied cell thicknesses and backside contact effects.

Annealing of Radiation Damage Effects

Further conceptual effort and evaluation of present studies with solar cells are desirable.

Modular Cell Group Fabrication

Refine present techniques being developed to allow the mass production of interconnected solar cells for large area panels. Such methods will reduce total array costs.

Pulsed Illumination for Panel Electrical Tests

Recent developments in this method of test are applicable to solar panels requiring large area illumination with excellent uniformity. Application of this method to high voltage solar panels with integral electronic should be explored.

Software Development — Specific Mission Optimization of Panel Configuration

The initial software for optimization of the array developed under this study should be continued. It promises a sophisticated and efficient method of high voltage array design.

APPENDIX A. RADIATION DEGRADATION CALCULATIONS

Two environmental conditions were considered for this analysis:

- 1) During ion engine powered orbit, the satellite will pass through the heart of the Van Allen radiation belts.
- 2) Following injection into synchronous orbit, the satellite will be exposed to solar proton activity and to synchronous trapped electron environment.

It was assumed that:

- 1) The initial altitude is 500 km
- 2) The acceleration due to the ion engine is constant.
- 3) The atmospheric drag decreases with altitude.
- 4) Ninety-one days are required to reach synchronous orbit.

From these conditions, a plot of altitude versus time was obtained.

The Hughes radiation environment computer program integrates elliptical orbits through the Van Allen belts to determine solar cell degradations. Since this particular trajectory is not elliptical, it was necessary to approximate the orbit raising trajectory. Five elliptical orbits were chosen as representative of the required trajectory. These orbits are shown in Table A-1. The number of days the satellite spends between the perigee and apogee altitude of each elliptical orbit is also given.

The synchronous equatorial radiation environment includes trapped electrons and solar flare protons. A launch date of 1972 and a period of 5 years in synchronous orbit were used for these calculations. The 1972-76 time period is expected to be nearly free of solar activity. The Hughes model predicts three solar proton events during this period as well as providing the nominal fluence for these events. The fluence due to the trapped environments (both the synchronous and lower altitudes) are calculated from maps of the Van Allen belts supplied by NASA.

TABLE A-1. REQUIRED TRAJECTORIES

Perigee Altitude		Apogee Altitude		Days Satellite is Between Perigee and Apogee Altitudes
Nautical Miles	Kilometers	Nautical Miles	Kilometers	
270	500	2,000	3,706	28
2,000	3,706	4,000	7,412	18
4,000	7,412	7,000	12,970	16
7,000	12,970	12,000	22,240	16
12,000	22,240	Synchronous	Synchronous	13

The calculations described above result in equivalent effective 1 mev electron fluences which are dependent upon coverslide thickness. The initial calculations are for front side radiation only (i. e., assume infinite backshielding).

Backside effects are included as follows. Solar cell response to backside radiation is not as well defined as response to front side radiation. Data from limited tests have indicated that a part of the solar cell thickness can be assumed to act as a shield (similar to coverslides). Only this layer of bulk material, and the thin substrate, will shield the high voltage array from backside radiation. For solar cells which are 0.015 cm (6 mils) thick, it was assumed that the cell bulk material and the substrate will provide approximately the same shielding as a 0.015 cm (6 mil) thick coverslide. Under these conditions, the equivalent front side fluence is doubled to determine the proper total fluence for use in degradation calculations. It should be stated that Hughes is planning a flight experiment for ATS-F that includes an investigation of backside radiation effects.

The authors of the NASA environments have indicated that these fluence levels are uncertain by approximately a factor of two. This uncertainty has been interpreted by Hughes to be equivalent to a 3σ limit. Calculations for this mission have indicated that the total solar flare contribution to the total fluence is insignificant compared with the Van Allen belt contribution. Therefore, the nominal fluences were multiplied by two to obtain 3σ equivalent electron fluences, without further consideration for the uncertainties of the solar proton model. Solar flare contribution has been included for the assumed launch date of 1972 in the illustration of degradation as a function of injection altitude (Figure 18, in Section 3).

APPENDIX B. DESIGN PRINCIPLES – STUDY I

The following design principles and decisions were developed during the High Voltage Array Study, Contract NAS 3-11535. They were applied in configuring the array models for the current study. They are presented here for reference and are not redeveloped in detail. Additional information is available in the High Voltage Solar Array Study (Reference 1) under the referenced contract.

A. Environment

1. Plasma

- a) Current losses are severe only for the highest positive voltages in the ionosphere. No special devices are required for voltages < 2000 volts in the ionosphere.
- b) Current losses may be reduced with the aid of suggested devices for high voltages in the ionosphere.
- c) Pinhole effects may be avoided with the aid of plasma collectors.
- d) Current losses, at an acceptable level, are treated as quasi-static loads.

2. Thermal

- a) Dielectrics are sized for the maximum predicted operating temperature.

3. Particulate Radiation

- a) Backside particulate radiation effects on solar cells must be considered for element sizing and performance predictions.
- b) The design point for a given dielectric in terms of radiation effects may occur prior to the end of life.

B. Materials

1. Passive

a) Dielectric failure

- (1) Bulk and surface failure to the plasma are not catastrophic if the mechanical integrity of the array is unaffected.
- (2) Bulk and surface failures between active elements are catastrophic.

b) Voids

- (1) Voids are permitted to exist in some cases.
- (2) Voids contributing to thru failures to the plasma are not catastrophic.
- (3) Voids between active elements are unacceptable.

c) Dielectric sizing

- (1) Required thickness depends upon emission discharge potential; such discharge occurs at 50 to 100 percent of commonly measured dielectric strength.
- (2) Designed to maximum beginning of life voltage in terms of:
 - (a) Substrate and
 - (b) Coverslide and
 - (c) Cell and bus spacingfor in-air ambient testing.
- (3) Out of eclipse condition is not used for sizing, shorting and isolation is employed.
- (4) Maximum temperature is chosen to fix thickness.
- (5) Sizing for radiation effects may be fixed by a rad. value prior to end of life.
- (6) Safety factor of two is assumed.

d) Material choices

- (1) Dielectrics resistant to the formation of residues in the presence of electrical discharge.
- (2) Transparent dielectrics and adhesives to allow void inspection.

- e) There is no need to control voltage gradients through cell group arrangements (ex. checkerboard pattern).
- f) A backside conductive grid is the only device employed that is foreign to conventional low voltage arrays.
- g) An initial outgassing period will be allowed in space prior to array turn-on.

2. Active

- a) Solar cell — coverslide
 - (1) Solar cell — Fabrication feasibility limited to 0.015 cm (6 mil) cell
 - (2) Minimum coverslide for dielectric requirements — 0.015 cm (6 mil)
- b) Bypass diodes
 - (1) Required for protection from open circuits.

C. Manufacturing

1. Fabrication

- a) Sequential order, segments are joined together to form panels.
- b) Stringent controls on cleanliness and inspection are required.
- c) Spacing of conductors for in-air testing allows eased tolerances in fabrication.

2. Testing

- a) Dielectrics are sized for in-air testing.

3. Safety

- a) Establishment of "safe" current levels.
- b) Shorting and isolation of cell groups during the fabrication procedure at the time of segment "joining".

D. Failure protection

1. Opens

- a) Higher probability of occurrence for a series string than for normal low voltage arrays.

2. Shorts

- a) Less probable

3. Design compensation

- a) Bypass diodes
- b) Blocking devices
- c) Transverse cell layout
- d) Clamping and isolation
- e) Out of eclipse
- f) Fabrication
- g) Backside grid

E. Pacing design principle

Any low voltage array may be employed for high voltage operations with only minor modifications.

APPENDIX C. SOLAR ARRAY OPTIMIZATION PROGRAM FOR SPECIFIC MISSION REQUIREMENTS

This program uses an iterative approach to optimally select two levels of current and voltage for sizing basic solar cell blocks. Any number of simultaneous loads may be considered, and there is no assumed limit to solar cell size. Block sizes are selected such that the total number of blocks used for all loads is a minimum for a specified load coverage capability.

Greater precision can be gained by decreasing the step size in statements 165 and 180. This will, however, significantly increase running time.

DEFINITION OF VARIABLES

Data

X1	=	Number of simultaneous loads
A(X)	=	Load values (in current or voltage)
G	=	Minimum allowable total load coverage
G3*	=	Minimum allowable coverage of total load by larger blocks
Il*	=	Maximum value (in current or voltage) of larger blocks

Print

G	=	Minimum allowable total load coverage
G1	=	Total load coverage by larger blocks
G2	=	Total load coverage by smaller blocks
Il (or V1)	=	Value of larger blocks

*These values are used only to limit program running time.

N1 = Number of larger block increments for given coverage (G1)
 I2 (or V2) = Value of smaller blocks
 N2 = Number of smaller block increments for given coverage
 (G2)
 S(1) [or S(V)] = Total load value

```

100  Read X1
110  Let A(0) = 0
120  For X = 1 to X1
130  Read A(X)
140  Let A(0) = A(0) + A(X)
150  Next X
160  Read G, G3, I1
165  For G = G to 0.995 Step 0.005
170  Let Y = 1E5
180  For G1 = G3 to 0.995 Step 0.010
190  Let G2 = (G - G1)/(1 - G1)
200  Let I = I1
210  Let W = 0.01*I
220  Let Q(0) = 0
222  If I <= 0 then 580
230  For F = 1 to X1
240  Let Q(F) = INT[A(F)/I]
250  Let Q(0) = Q(0) + Q(F)
260  Next F
270  Let J = Q(0)*I/A(0)
290  If J >= G1 then 312
294  Go to 300
300  Let I = I - W
310  Go to 220
312  If G2 <= 0 then 460
320  Let O = I
330  Let R(0) = 0
340  Let K(0) = 0
350  For M = 1 to X1
360  Let K(M) = A(M) - Q(M)*I
370  Let K(0) = K(0) + K(M)
380  Let R(M) = INT[K(M)/O]
390  Let R(0) = R(0) + R(M)
400  Next M
410  Let T = 1
420  Let N = R(0)*O/K(0)
430  If N >= G2 then 460
440  Let O = O/(T + 1)
450  Go to 330
460  Let C = 0
470  Let D = 0
480  For P = 1 to X1
  
```

```

500   Let C = C + Q(P)
510   Let D = D + R(P)
512   If G2 <= 0 then 516
514   Go to 520
516   Let D = 0
520   Next P
530   If Y < C + D then 570
532   For R1 = 0 to X1
534   Let Z(R1) = Q(R1)
536   Let H(R1) = R(R1)
538   Next R1
540   Let Y = C + D
550   Let Y1 = C
560   Let Y2 = D
562   Let Z1 = I
564   Let Z2 = O
566   Let Z3 = G1
568   Let Z4 = G2
570   Next G1
580   Let S = (Z1*Y1 + Z2*Y2)/A(0)
590   Print "G="G, "G1="73, "G2="74
600   Print
610   Print
620   If Z1 > 1.0 then 820
630   Print "I1="71, "N1="Y1
640   Print
650   Print
660   Print "I2="72, "N2="Y2
670   Print
680   Print
690   Print "(I1*N1 + I2*N2)/S(I) ="S
692   Print
694   Print
696   Print "I", "N1(I)", "N1(I)*I1", "N2(I)", "N2(I)*I2"
698   Print
700   For R1 = 0 to X1
702   Print A(R1), Z(R1), Z(R1)*Z1, H(R1), H(R1)*Z2
704   Print
706   Next R1
710   Print
780   Print "*", "*", "*", "*", "*"
790   Print
800   Print
805   Next G
810   Go to 100
820   Print "V1="Z1, "N1="Y1
830   Print
840   Print
850   Print "V2="Z2, "N2="Y2
860   Print
870   Print

```

```

880 Print "(V1*N1 + V2*N2)/S(V)='S
882 Print
884 Print
890 Print "V", "N1(V)", "N1(V)*V1", "N2(V)", "N2(V)*V2"
892 Print
894 For R1 = 0 to X1
896 Print A(R1), Z(R1), Z(R1)*Z1, H(R1), H(R1)*Z2
898 Print
900 Next R1
902 Print
904 Print "*", "*"  "*", "*", "*"
906 Print
908 Print
910 Go to 805

```

APPENDIX D. THERMAL ANALYSIS OF SOLAR PANEL MOUNTED ELECTRONICS

A parametric thermal analysis to aid in evaluating problems associated with placing solid state electronics on the solar panel has been completed. The problem consisted of determining design parameters for heat dissipating, integrated electronics mounted on a solar array (see Figure D-1). The design requirement was to make the package small, thereby utilizing the least possible solar panel surface area while maintaining acceptable electronics temperatures. The orbital altitude of the satellite was assumed to range from 500 km (270 n.mi.) to high altitude synchronous orbit. A sketch of the solar panel and electronics geometry with respect to the earth and sun at several orbital positions is shown in Figure D-2.

Four different thermal configurations were analyzed. They consisted of various combinations of silver quartz mirrors, aluminized teflon, and aluminized kapton on the front and back surfaces of the electronic package. The thermal configurations studied are summarized in Table D-1, along with the solar absorptivities and infrared emissivities used in the analysis for each material.

The following three orbital environments were analyzed for each design:

- 1) High altitude synchronous orbit (no reflected solar or infrared earth heat backloading)
- 2) Low altitude orbit (500 km) at the maximum heat loading subsolar point position ($\theta = 0$ degree, in Figure D-2).
- 3) Low altitude orbit, but with incident direct solar, reflected solar, and IR earth heat loads averaged over one complete earth orbit.

Steady state calculations were made for each of these external heating conditions. Because of the constantly changing external heat loads during a low altitude orbit, steady state temperatures corresponding to the maximum heat load condition at low orbit will not be reached. Therefore, the second environment bounds the maximum temperatures reached by the electronics at 500 km altitude. The third environment is a lower bound for the maximum unit temperature at 500 km altitude when capacitance effects are ignored. It corresponds to an average temperature for the electronics package during a complete orbit at low altitude.

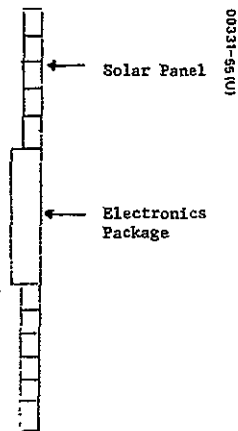


Figure D-1. Cross Section of Solar Panel and Electronics Package

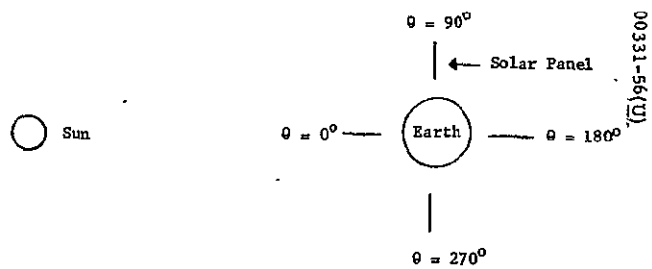


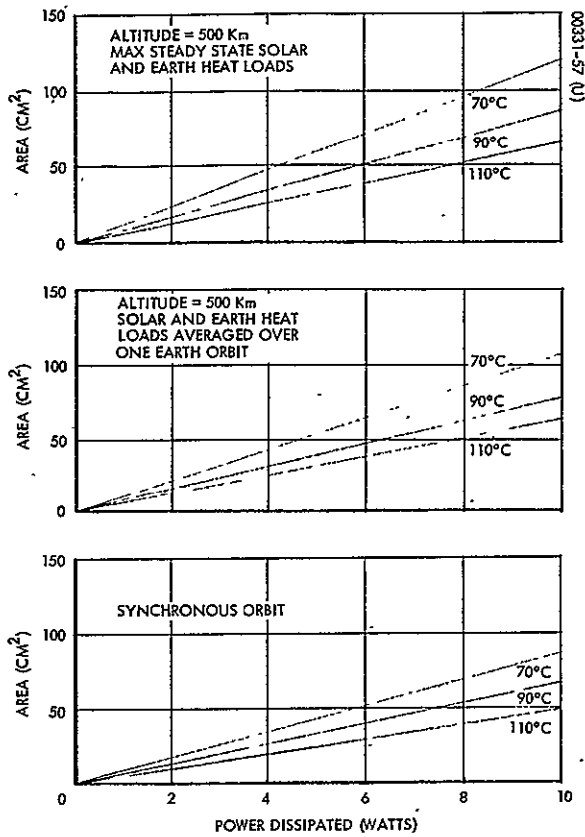
Figure D-2. Solar Panel Orientation

TABLE D-1. THERMAL CONFIGURATIONS ANALYZED

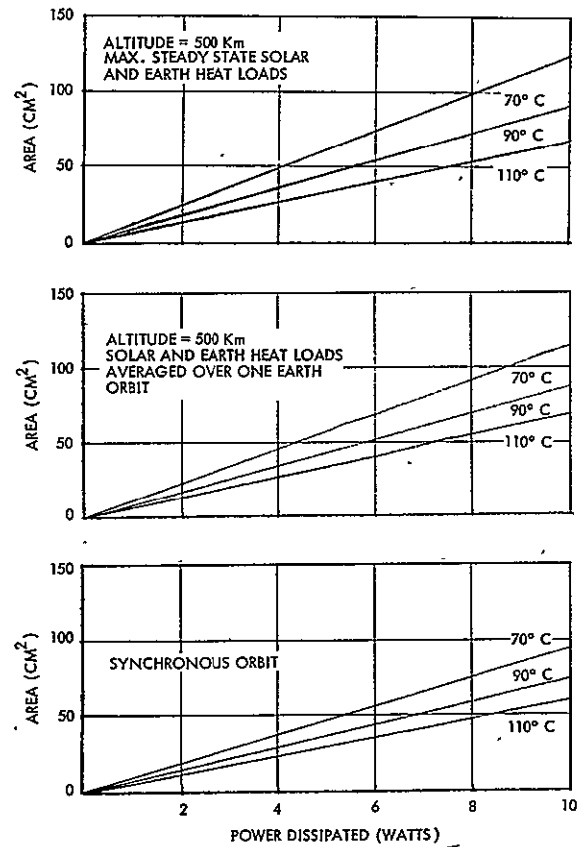
Configuration	Silver- Quartz	Aluminum- Teflon	Aluminum- Kapton
1. Solar illuminated exterior Non-solar illuminated exterior	X		X
2. Solar illuminated exterior Non-solar illuminated exterior	X	X	
3. Solar illuminated exterior Non-solar illuminated exterior		X	X
4. Solar illuminated exterior Non-solar illuminated exterior		X X	
Thermal Properties Assumed			
Material	Solar Absorption	IR Emissivity	
Silver-quartz mirrors	0.07	0.8	
0.005 cm (2 mils) aluminized teflon	0.25	0.65	
0.013 cm (5 mils) aluminized kapton	0.4	0.8	

Results for each thermal design at the several orbital conditions are illustrated in Figure D-3. Each graph shows the necessary electronics area as a function of internal heat dissipation to maintain the package at a particular temperature. Calculations were made to maintain package temperatures at 70°, 90°, and 110° C.

It appears that the least solar panel area will be taken up if the electronics package has quartz mirrors on the solar illuminated exterior and aluminized kapton on the non-solar illuminated exterior.

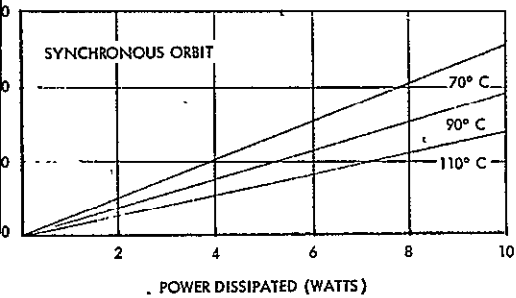
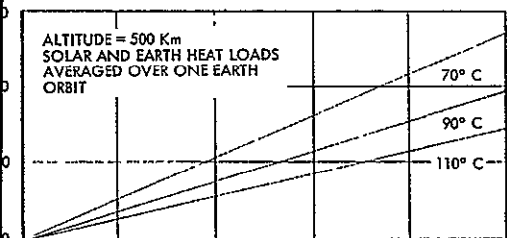
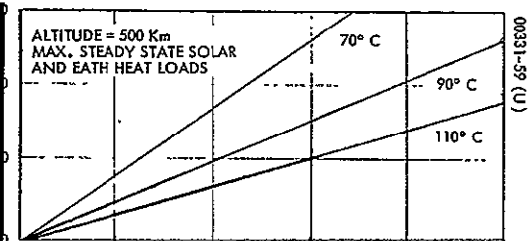


a) Configuration 1

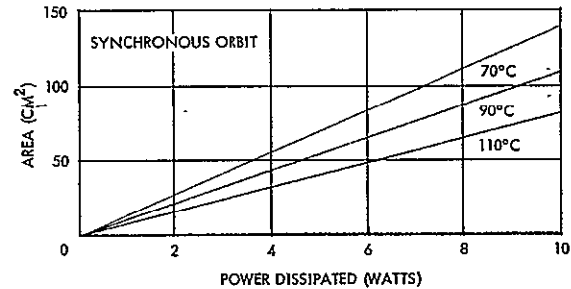
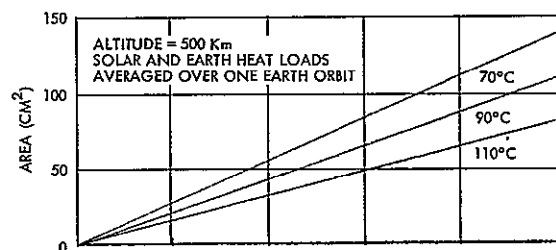
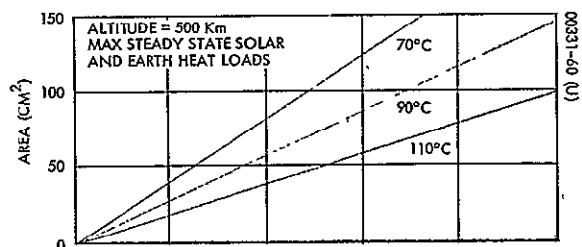


b) Configuration 2

Figure D-3. Required Area Versus Power Dissipated for
Solar Panel Mounted-Electronic Unit



c) Configuration 3



d) Configuration 4

APPENDIX E. RELIABILITY ANALYSIS

This appendix presents a condensation of the reliability analysis performed. To minimize the duplication of various figures and written material, originally a part of the analysis discussion, occasional reference will be made to the main body of the report.

The reliability analysis and reliability modeling conducted for the High Voltage Solar Array Configuration Study has concentrated on those factors unique to such a power system. This has included determining the trends in solar array reliability as a function of its subdivision into individual sectors or blocks of solar cells, establishing the effectiveness of various regulation schemes to provide smooth regulation with minimal power loss and assessing the problems associated with reconfiguration switching.

The following comments and conclusions are pertinent to the analysis.

- 1) The reconfiguration switches and the high voltage isolation between switch elements and control signals represent the two major device related reliability problem areas.
- 2) Projected desired reliabilities for reconfiguration switches in the more versatile switching arrangements exceed that presently achievable for known solid-state type switches, power transistors, silicon controlled rectifiers, etc. The failure rates of high voltage vacuum relays appear acceptable if the number of operations is low.
- 3) In general, simple reconfiguration arrangements with low power losses per switch failures are preferred over highly versatile arrays. Any increase in the number of switches should be used to increase the reliability of a single switch position through switch redundancy rather than by increasing power routing paths.
- 4) Regulation schemes which have redundant low voltage sections with single switch elements and redundant switches for high voltage sectors appear preferred for achieving smooth regulation with minimal power loss.

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- 5) The critical level of a switch (regulation or reconfiguration) is proportional to the power lost due to its failure; hence, the failure probability of a switch should be inversely proportional to the power controlled by the switch.
- 6) The reliability of the solar cell power can be maintained at the required value after subdivision into low current power units with moderate weight and area penalties, by using bypass diodes or cells with soft back biased characteristics.

FUNCTIONAL RELIABILITY PROGRAM

The following major functions, subsystems, and components were considered in performing the reliability analysis and modeling.

- 1) Unregulated solar array sections
- 2) Hard-wired interconnect lines
- 3) Regulation/control switches
- 4) Reconfiguration switches
- 5) Switch control lines
- 6) Isolation between switches and control signals
- 7) Control logic electronics
- 8) Sensing and error detection
- 9) Isolation between sensing and control electronics
- 10) Programmer and command decoder

To simplify the analysis and the structuring of a reliability model which concentrates on the unique reliability aspects associated with reconfigurable high voltage arrays with integral power conditioning, the above listed items will be further combined into the designated functions: solar cell array, regulation, reconfiguration, and control.

Solar Cell Array

The solar cell array is subdivided into configured hard-wired solar cell sections or blocks. The I-V characteristics of these power units can be modified by the regulation switches when the switches are appropriately attached to internal points in the block. The reliability associated with the solar array is the ability of the solar cells to produce rated power, hence, is dependent on the reliability of the solar cell, bypass and blocking diodes, and associated permanent hard-wired interconnect lines.

Regulation

The regulation functional unit is composed of switches which are activated (driven ON or OFF) by the control unit to maintain the proper output levels to each load. The reliability of each switch has associated with it the reliability of the isolation between the switch element and the control signal, and the reliability of the control line.

Reconfiguration

This unit contains the reconfiguration switches which provide for combining in series, parallel, and/or series-parallel fashion the solar array sections and routes the resultant power to the appropriate loads. The reliability of each switch in the reconfiguration arrangement (as with regulation switches) has associated with it the reliability of the isolations between the switch element and the control signal, and the reliability of the control line.

Control

The functional block designated as control is assumed to contain items (7) through (10). This unit receives signals (from ground command or on-board sensors) and acts by issuing control signals to the appropriate reconfiguration or regulation switches. Through proper design, this unit should have an external high reliability value and except for the possibility of requiring high voltage isolation for sensing, constitutes a low voltage logic design problem area.

A functional system reliability diagram depicting a series model is shown in Figure E-1. The reliability of the total system, R_{system} , is taken to be the product of the reliability of the individual functions. If the reliabilities of the solar cell array, regulation, reconfiguration, and control are denoted by R_1 , R_2 , R_3 , and R_4 , respectively, then

$$R_{\text{system}} = R_1 R_2 R_3 R_4$$

The value of $R_{\text{system}} = 0.99$ has been taken as a desirable reliability to be achieved by the high voltage solar array system. Because of uncertainties in projecting reliability values for a number of the components suggested for mechanizing the array concept (particularly in the areas of reconfiguration and regulation), most of the reliability effort concentrated on assessing problem areas and on analysis to support design decisions in choosing among various functional approaches.

Switches

The switches associated with either the functions of regulation or reconfiguration can be modeled in the following way. Let

- R_{CL} = The reliability of the control line from the point the control signal is initiated to the active switch element.
- R_{SI} = The reliability of the electrical isolation between the control signal and the active switch element. This isolation may be achieved, for example, by isolation transformers or some form of photo-optical methods.
- R_{SE} = The reliability of the switch element. The element is the actual physical portion which controls current flow, and may correspond to a mechanical relay contact or some solid-state device.

The reliability of a switch to achieve both the open (OFF) and closed (ON) function will be denoted by R_{SW} . It follows that

$$R_{SW} = R_{CL} R_{SI} R_{SE}$$

The relative failure rates for either open-circuit or short-circuit switch failure modes can be determined from the specific device configuration employed. In order to discuss in the following sections means of achieving switching redundancy, it will be helpful to establish failure mode terminology here. Let

f_{SWO} = The open-circuit failure probability

f_{SWS} = The short-circuit failure probability

Then

$$f_{SW} = f_{SWO} + f_{SWS}$$

denotes the failure probability and

$$R_{SW} = 1 - f_{SW}$$

Typically, the switch element will dominate in determining the switch reliability such that $R_{CL} \gg R_{SE}$ and $R_{SI} \gg R_{SE}$, hence

$$R_{SW} \approx R_{SE}$$

For a first evaluation of high voltage solar array reliability potential, this approximation is sufficient. An additional point to remember is that the failure of the high voltage isolation of a single switch (either a switch for regulation or reconfiguration) may have an undesired effect on the low level logic circuitry controlling a major portion of the power system. It appears advisable even at this conceptual stage to propose that the double (or cascaded) high voltage isolation be incorporated in the design. A typical application of this would be isolation at the point the control signal is generated and again at the switch element interface. The center section of the control path could then be established at a given potential.

SOLAR CELL ARRAY

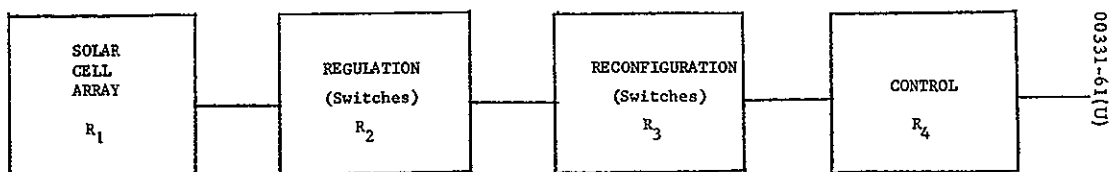
A discussion of open circuit failure protection using bypass diode is given in Section 3 of the main text. The figures presented there (Figures 9 and 10) display the most likely or expected percentage of bypassed groups and gives an optimistic estimate of the percent oversizing that must be provided in order to achieve the designated power level (15 kw) at end-of-life with a probability of 0.99.

The result can be extended to establish a curve which for a given probability projects the upper percentage of bypassed groups as a function of the number of cells in parallel. Then, if the array is oversized to the upper percentage, the reliability of the solar cell array is equal to the given probability.

Without regard to bypass-diode and block-spacing area penalties, it is desirable (from the standpoint of reliability and output flexibility) to configure power units with a bypass diode per row (or use cells which have a back biased characteristic closely approximating that of a forward biased diode) and with a minimum of cells in parallel if less than eight. When this approach is taken, the upper percentage of groups bypassed (row failures) with probabilities 0.995+ and 0.999+ are represented by the curves in Figure E-2 for the range of 1, 2, and 3 cells per bypassed row. These latter subdivisions correspond to the block sizing for the universal array model.

The percentage of array power oversizing required to achieve the array power reliability can be determined from the curve once the blocks are chosen. Care must be taken when determining the power sizing to consider not only the power generation lost, but also the voltage drop in the bypass diode; i. e., typically, the loss of a single row through bypass can constitute a power loss in excess of three times the power that the row was generating.

The curves were generated using the bimonial distribution assuming a large number of series rows, hence they typify the reliability performance of high voltage (≥ 500 volt) blocks. In later sections, when considering the reliability of various regulation schemes, the reliability of low voltage sectors in the range of a few volts to 200 volts is needed particularly to assess the relative reliabilities of the sectors of voltage and their associated regulation switches.



$$R_{\text{system}} = R_1 R_2 R_3 R_4$$

Figure E-1. System Reliability Diagram

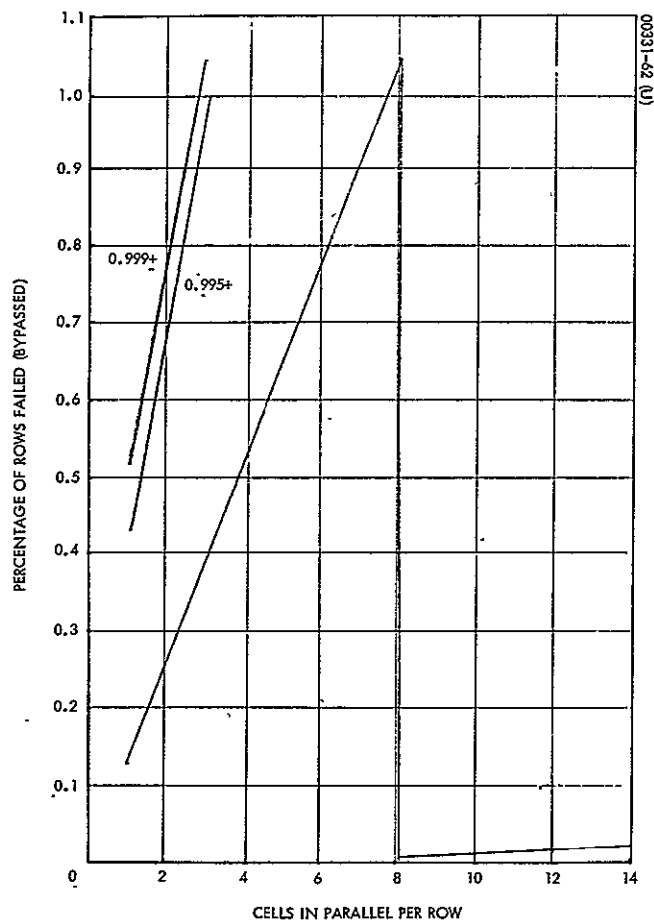


Figure E-2. Row Failure (Bypass) Rate as a Function of Number of Cells in Parallel

Assume that the i^{th} voltage sector is composed of n_i rows (each row bypassed with a bypass diode) and that each row contains m_i cells; i. e., the sector is composed of $n_i \times m_i$ cells. For $m_i < 8$ (standard 2×2 cm cells), a row will go in bypass if at least one of the cells opens. If the sector continues to provide the same current, the voltage loss will be $v_d + v_c$, where v_d is the bypass diode drop and v_c is the voltage of a single row at the given current. The total voltage of a single sector prior to a row failure is $n_i v_c$ and the voltage after $n_i v_c - (v_d + v_c)$. Letting $v_d + v_c = v_{dc}$, the voltage after r failures is:

$$v_i(r) = n_i v_c - r v_{dc}$$

The reliability of this voltage sector (considering only solar cell failures) can be presented in terms of the number r or

$$R_{SC_i}^{(r)} = \text{Prob} (\leq r \text{ rows are bypassed in the } i^{\text{th}} \text{ sector})$$

With $m_i < 8$

$$R_{SC_i}^{(r)} = \text{Prob} (\leq r \text{ rows have at least one open cell failure in the } i^{\text{th}} \text{ sector})$$

Now, the open circuit failure probability of a single cell will be denoted by f_c and its value was previously given as 0.001314. The failure probability of any row ($m_i < 8$) can be taken as

$$f_r \simeq m_i f_c$$

Hence, it follows that

$$R_{SC_i}^{(r)} = \sum_{k=0}^r \binom{n_i}{k} f_r^k (1 - f_r)^{n_i - k}$$

For a binary weighted system, a typical sequence of n_i cells might be given by

$$5, 10, 20, 40, 80, 160 \dots$$

Then, the probability of zero bypassed rows, $R_{SC_i}^{(0)}$ can be represented by the following approximate tabulation.*

TABLE E-1. $R_{SC_i}^{(0)}$

$n_i \backslash m_i$	1	2	3	4
5	0.994	0.987	0.980	0.974
10	0.987	0.974	0.961	0.948
20	0.974	0.948	0.922	0.900
40	0.948	0.900	0.845	0.811
80	0.900	0.811		
160	0.811			

These values show that locally the probability that a given sector will provide its nominal design value can become quite small. Nevertheless, the important question is whether the relative output levels of the individual sectors (for fixed m_i) show sufficient invariance to produce a smooth ramp transfer characteristic for regulation.

Since $R_{SC_i}^{(r)}$ can increase so rapidly with increasing r , particularly for large n_i , it is more logical to give a qualitative assessment of the parameter R_{SC_i} found in the regulation section. A single row bypassed in the lower voltage sections can greatly influence the smoothness of control of the output voltage or current unless redundant equally weighted sections are provided. Hence, their influence on the regulation capability must be judged basically on the probability of no rows lost or the probability of maintaining the designed voltage weighting. The larger sectors have increasingly less influence (the largest has none) on the smoothness of control, and primarily only influences the range of control. In this case, $R_{SC_i}^{(r)}$ values for reasonable values of r ; i.e., for r values corresponding to 1 to 5 percent, voltage losses can be assumed to represent R_{SC_i} and for purposes of regulation analysis, their value approaches 1.

*For $r = 0$, $R_{SC_i}^{(0)} = (1 - f_c)^{n_i m_i}$

REGULATION

The functional aspects of the regulation subsystem are presented in detail in Section 4 of the main body of the text.

It is proposed that load regulation, current or voltage, be achieved by using switches to modify the I-V characteristics of groups of solar cells in discrete steps. Abstractly, this reduces to the problem of providing sufficient numbers of switches to remove up to ΔV volts. In order to satisfy the regulation specification, ΔV must be removed in small steps or in a weighted format, which produces an equivalent effect. A typical transfer characteristic denoting voltage removed as a function of the control signal level is shown in Figure E-3. The step size \bar{V} must be small enough with respect to the total output voltage to provide the required resolution.

From the standpoint of the reliability study, it is desirable to establish the control concepts which:

- 1) Provide a smooth regulation characteristic with no discontinuities greater than \bar{V}
- 2) Lead to the smallest expected power loss due to failures of the regulation switch elements

The above two factors are often in opposition. In addition, a large number of switches will lead to greater control line and control logic complexity.

Two means of voltage removal have been considered. These have been classified as the series removal and shunt removal techniques. They are discussed in detail in subsection 4.2 of the text.

For each of the concepts, the reliability model is essentially the same. If the reliability of the i th weighted sector of solar cells is denoted by R_{SC_i} and if the switch associated with this sector (for either the series or shunt concept) is given by R_{SW_i} , then the equivalent reliability of each sector is

$$R_{S_i} = R_{SC_i} R_{SW_i}$$

This reliability equals the probability that at the end of the mission, the i th sector is producing a voltage within a given range at a specified current and that the sector can be switched to provide regulation.

A large number of sector voltage weighting schemes were considered, ranging from binary weighting to single weighted systems where the voltage ΔV is removed in equal steps \bar{V} . In addition, various orders of redundancy (or partial redundancy) of the weighted sectors were investigated. The general conclusion reached was that sector weighting requiring fewer switches and having partial redundancy of the lower voltage sectors leads to an optimum approach.

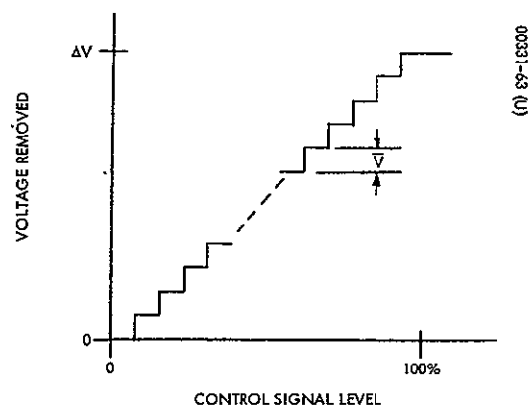


Figure E-3. Regulation Transfer Characteristics

Reliability Equations for a Block of Power

Let R_R denote the probability of perfect regulation. For a system with N sectors, none of which are redundant, all sectors must function properly to provide regulation of the required smoothness \bar{V} and range ΔV , hence.

$$\begin{aligned} R_R &= \prod_{i=1}^N R_{S_i} \\ &= \prod_{i=1}^N R_{SC_i} R_{SW_i} \\ &= \prod_{i=1}^N R_{SC_i} (1 - f_{SW_i}) \end{aligned}$$

For those cases where the weighting of the sectors does not constitute a major difference in the stress placed on each of the switches, the above becomes

$$R_R = (1 - f_{SW})^N \prod_{i=1}^N R_{SC_i}$$

Since it is desirable to grade different regulation schemes, it is worthwhile to consider other facets related to reliability, particularly the expected power loss for each scheme due to the inclusion of the switch; i. e., the expected power loss P_L due to switch failures without regard to solar cell failures. Let $E(X)$ denote the expected value of X where X is a random variable or sum of random variables. Assume that the N sector voltages, V_i , $i = 1, \dots, N$, sum (with no switch failures) to ΔV ; i. e.,

$$\Delta V = \sum_{i=1}^N V_i$$

Then the expected end-of-life power loss (which can be directly related to voltage loss) is, at a given current level I , given by

$$E(P_L) = \left(\sum_{i=1}^N \tilde{f}_{SW_i} V_i \right) I$$

where \tilde{f}_{SW_i} is the failure probability of the mode which causes a loss of power. Recall that for regulation, it has been assumed that the switch must be able to assume either the open or closed state. Hence, in evaluating the above equation

$$\tilde{f}_{SW_i} = f_{SWO_i}$$

for the series method of voltage removal and

$$\tilde{f}_{SW_i} = f_{SWS_i}$$

for the shunt removal technique.

Comparison of Regulation Schemes

In the following sections, five regulation schemes will be studied in some detail. The equations depicting regulation reliability and expected power (voltage) loss will be presented and a gross evaluation of the merits of the techniques will be given.

The functional block diagram representing the subdivision of the block of power are shown in Figures 32 and 33 of the main text. For concreteness, the voltage weighted format is assumed to be binary, since this leads to the minimum number of switches to achieve any removal objective. The equations and related reliability block diagrams are, however, applicable to most voltage weighted schemes. All switches are assumed to have a pre-dominate failure mode which causes a loss of power.

Straight Binary

For this regulation scheme, the describing equations previously developed hold without modifications, i. e. ,

$$R_R = \prod_{i=1}^N R_{SC_i} (1 - f_{SW_i}) = \prod_{i=1}^N R_{SC_i} R_{SW_i}$$

$$E(P_L) = \left(\sum_{i=1}^N \tilde{f}_{SW_i} V_i \right) I$$

If $\tilde{f}_{SW_i} = \bar{f}_{SW}$ for every i , then

$$E(P_L) = \left(\bar{f}_{SW} \sum_{i=1}^N V_i \right) I = \bar{f}_{SW} \Delta V I$$

Here the range of N might typically be 8 for a ΔV of 255 volts in steps of 1.0 volt. The value of R_R is relatively low, since each of the sectors must be operative to achieve a smooth regulation characteristic. For the example voltage of 255 volts, the sector sequence would be

1, 2, 4, 8, 16, 32, 64, 128

At best, the loss of any sector would be equally likely so that the loss of 128 volts is as likely as the loss of 1 volt. The maximum current rating of the switches to achieve regulation would be equal to the total short circuit current, I_{SC} .

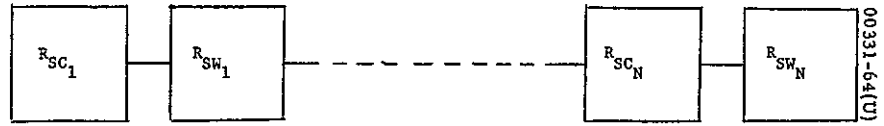
The block diagram reliability model denoting this scheme is shown in Figure E-4.

M Fold Binary: Voltage Division

For $M = 1$, this scheme corresponds to the straight binary and can be extended to $M = 255$ (for example voltage) leading to 255 1.0 volt sectors. Basically, the scheme divides ΔV into M equal voltage sections where each section is again divided into binary weighted sectors. For $M = 4$, the following sequence is applicable (for 252 volts):

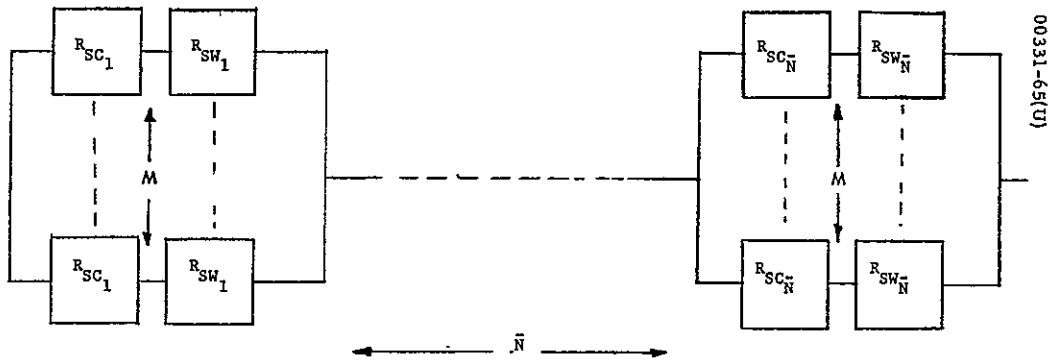
1, 2, 4, 8, 16, 32
1, 2, 4, 8, 16, 32
1, 2, 4, 8, 16, 32
1, 2, 4, 8, 16, 32

This requires 24 switches, each with a maximum current rating of I_{SC} (I_{SC} equals the maximum short circuit current associated with I). The smoothness of regulation is assured if any one of M switches is operative for each weighted sector. Any switch failures will, of course, effect the range of control and expected losses. The block diagram reliability model for this scheme is shown in Figure E-5 and the describing equations are given below.



$$R_R = \prod_{i=1}^N R_{SC_i} R_{SW_i}$$

Figure E-4. Reliability Model - Straight Binary



$$R_R = \prod_{i=1}^{\bar{N}} [1 - (1 - R_{SC_i} R_{SW_i})^M]$$

Figure E-5. Reliability Model - M Fold Binary, Voltage Division

Let \bar{N} denote the number of differently weighted sectors. Then, returning to the original describing equation for R_R ,

$$R_R = \frac{\bar{N}}{\pi} R_{S_i}$$

Since regulation smoothness exists if at least one sector of each weight is functional,

$$\begin{aligned} R_{S_i} &= \text{Prob (1 out of } M \text{ of the } i^{\text{th}} \text{ weighted sectors is functional)} \\ &= 1 - \left(1 - R_{SC_i} R_{SW_i}\right)^M \end{aligned}$$

hence

$$R_R = \frac{\bar{N}}{\pi} \left[1 - \left(1 - R_{SC_i} R_{SW_i}\right)^M \right]$$

where $M \cdot \bar{N}$ is the total number of sectors (total number of switches). It follows that

$$E(P_L) = M \left(\sum_{i=1}^{\bar{N}} \tilde{f}_{SW_i} V_i \right) I$$

Again, if $\tilde{f}_{SW_i} = \bar{f}_{SW}$ for every i , then

$$E(P_L) = \bar{f}_{SW} \Delta V I$$

which is the same as for the straight binary system.

M Fold Binary: Current Division

This scheme uses the same voltage sector weighting as for the straight binary system. Here, however, the current capability is subdivided into M equal strings of I/M . The total number of sectors (switches) is MN . For the same ΔV as in the previous examples and $M = 3$, the number of switches becomes 24, or the same number as for the voltage division scheme with $M = 4$.

One of the major advantages of this scheme is that the current rating of the switches is reduced considerably and can be of benefit for switches physically placed on the array. This has been achieved at the expense of requiring more bypass diodes (by at least a factor of M); however, the reliability R_{SC_i} is higher for the small sectors because of reduced m_i .

The block diagram reliability model is shown in Figure E-6 and is seen to be analogous to that for the voltage division system for $N = \bar{N}$ although there would be minor differences in the closed loop I-V characteristics in case of switch failures. The describing equations are:

$$R_R = \prod_{i=1}^N \left[1 - (1 - R_{SC_i} R_{SW_i})^M \right]$$

and

$$E(P_L) = M \left(\sum_{i=1}^N \tilde{f}_{SW_i} V_i \right) I / M = \left(\sum_{i=1}^N \tilde{f}_{SW_i} V_i \right) I$$

For $\tilde{f}_{SW_i} = \bar{f}_{SW}$ for every j

$$E(P_L) = \bar{f}_{SW} \Delta V I$$

This scheme again projects the same power loss as in the previous cases.

Straight Binary: Redundant Switches

As the name implies, this scheme employs voltage weighted sectors identical to the straight binary system, but uses additional switch elements in given configurations to reduce the failure probability of the predominate failure modes. The following cases exist:

- 1) If $f_{SWS} \gg f_{SWO}$, use series switch arrangements to improve effective switching reliability
- 2) If $f_{SWS} \ll f_{SWO}$, use parallel switch arrangements to improve effective switching reliability
- 3) If $f_{SWS} \approx f_{SWO}$, use series-parallel or parallel-series arrangements (typically Quads) to improve effective switching reliability

The area of switch element redundancy is considered again in the sections concerned with reconfiguration switches where a much larger power loss is associated with each switch function failure.

The following example is chosen to demonstrate (optimistically) the improvement that can be expected in the switch redundancy approach. Without loss in generality, let the shunt removal technique be used and assume that $f_{SW} = f_{SWS}$, $f_{SWO} = 0$. Across each voltage sector assume that M series switches are used such that the effective switch failure probability is

$$f_{SWS_i}^M$$

Then

$$R_R = \prod_{i=1}^N R_{SC_i} (1 - f_{SWS_i}^M)$$

and

$$E(P_L) = \left(\sum_{i=1}^n f_{SWS_i}^M V_i \right) I$$

The block diagram reliability model is shown in Figure E-7. If $f_{SWS_i} = \bar{f}_{SWS}$ for every i , then

$$R_R = \left(1 - \bar{f}_{SWS}^M \right)^N \prod_{i=1}^N R_{SC_i}$$

and

$$E(P_L) = \bar{f}_{SWS}^M \Delta V \cdot I = \bar{f}_{SWS}^{M-1} (\bar{f}_{SWS} \Delta V \cdot I)$$

Under the above assumption, it is concluded that large improvements in regulation, and particularly in the expected power loss, can be achieved by the switch element redundant approach. For the example voltage of 255 volts ($N = 8$), and $\bar{f}_{SW} \approx 0.01$, the expected power loss is reduced by a factor of 10^{-4} of its values for the nonredundant scheme when a total of 24 switches are used. If the control and control line reliability can be maintained sufficiently high, the redundant switch elements can be grouped and use a common signal, thereby reducing the system's complexity.

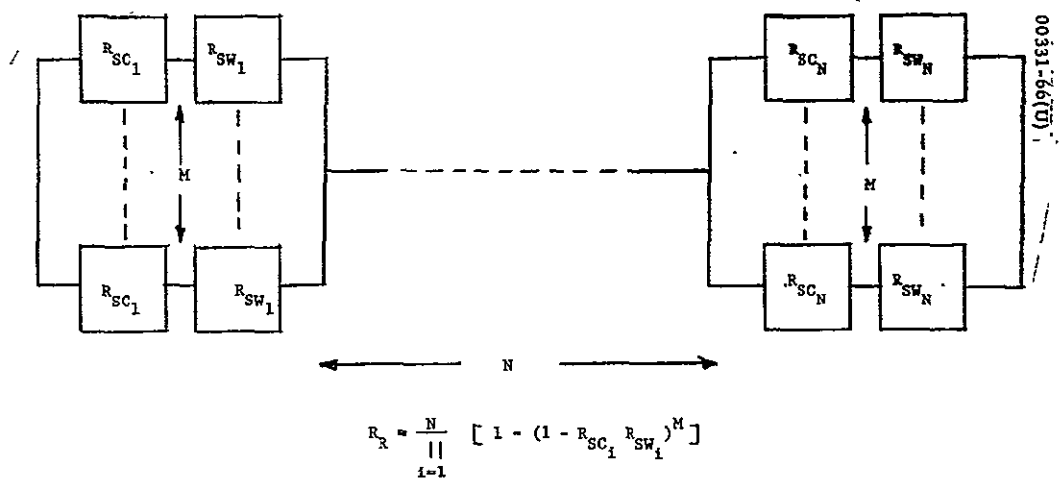


Figure E-6. Reliability Model - M Fold Binary, Current Division

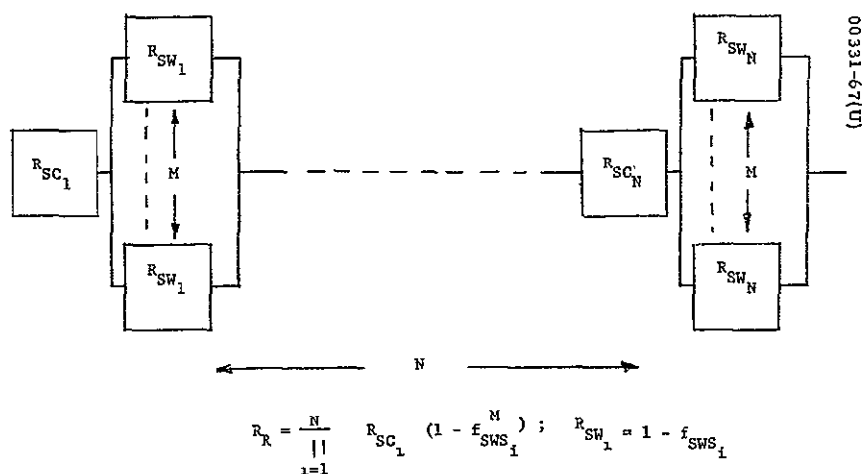


Figure E-7. Reliability Model - Straight Binary, Redundancy Switches

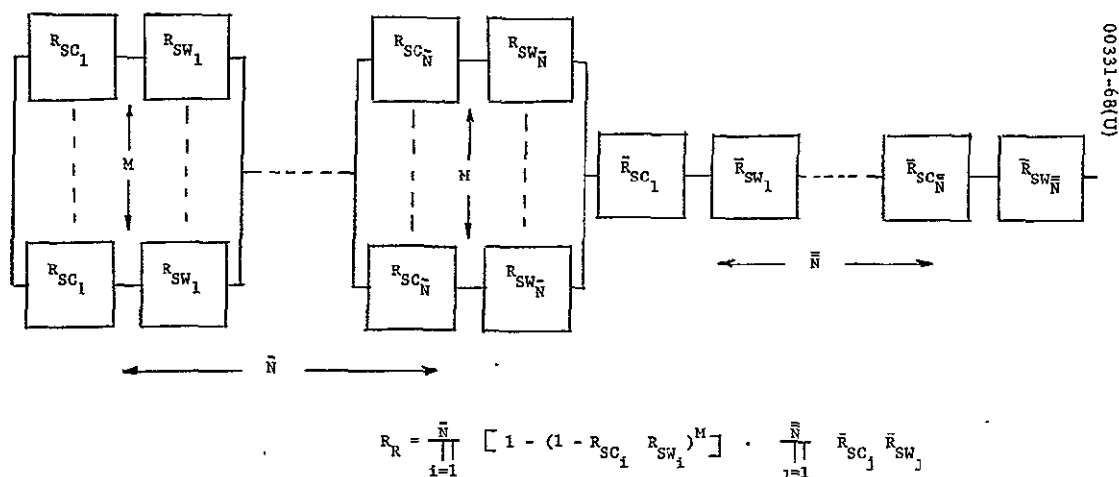


Figure E-8. Reliability Model - M Fold Binary, Voltage Division Plus Current Trimming

M Fold Binary: Voltage Division Plus Current Trimming

The functional block diagram depicting this approach for regulating a block of power (and extendible to the total control or regulation of combinations of controllable and uncontrollable blocks) is shown in Figure 33 of the main text. Basically, the concept depends on the unregulated current sections to provide for gross adjustments of the output and for the ΔV section to provide fine control. It is quite possible that these gross adjustments could be achieved by reconfiguration switches; however, for the present discussion, the switches are considered as regulation switches.

Various current weighting formats are possible. For example, binary weighted sections would provide the smoothest gross adjustments with the fewest switches (sections) and would allow the voltage removal regulation switches in the ΔV section to be sized for the minimum current, a possible major advantage.

The concept does not lend itself to a straightforward comparison with the previous concepts, although for the same size power block, approximately the same range of ΔV removal will be required. As with all previous techniques, it is possible that $\Delta V \equiv V$.

Let the subscript i identify the ΔV switches and voltage sectors, and let j denote quantities associated with the current trimming sections. The describing equations for this system are (assuming that the loss of any current string constitutes a loss of regulation)

$$R_R = \prod_{i=1}^{\overline{N}} \left[1 - (1 - R_{SC_i} R_{SW_i})^M \right] \cdot \prod_{j=1}^{\overline{N}} \overline{R}_{SC_j} \overline{R}_{SW_j}$$

and for the shunt method of voltage removal

$$E(P_L) = \sum_{i=1}^{\overline{N}} M \tilde{f}_{SWS_i} V_i I_i + \sum_{j=1}^{\overline{N}} \tilde{f}_{SWO_j} V_j I_j$$

See Figure E-8 for the block diagram reliability model. It is realistic to make the following simplifying assumptions: the current division is such that the ΔV section has current capability kI and the total capability of the current trimmer sections is $(1 - k)I$ for $0 < k \leq 1$. $V_j = V$, and

$$\tilde{f}_{SWO_j} = \tilde{f}_{SWO}$$

for every j . The above equation then becomes

$$E(P_L) = MkI \sum_{i=1}^{\bar{N}} \tilde{f}_{SWS_i} V_i + \tilde{f}_{SWO} V(1 - k)I$$

This concept has good potential for achieving high regulation reliability with low expected power loss. In addition, it should be a very applicable concept for wide range control or in configurations where an extra current string could be shared among many blocks to provide partial redundancy.

RECONFIGURATION

A discussion of the functional operation of various specific reconfiguration switching arrangements and the devices proposed to mechanize the arrangements are discussed in detail in Section 5 of the main text.

Most of the reliability effort in this area has been directed toward reviewing various reconfiguration concepts to assess the critical failure paths and the potential of each concept to reliably achieve the system objective. A detailed evaluation of the reliability of each power transfer path between solar array power and the load is beyond the scope of the present study. As work is continued past this early conceptual study, specific concepts can and must be analyzed in greater depth since the reconfiguration switching arrangement is judged the critical system area.

The basic device chosen to perform the individual switching functions can be modeled as previously discussed in the switch section, and the model of the reconfiguration arrangement can be represented as a series subsystem which conveys (combines and routes) the controllable (regulated) solar array power to the appropriate loads.

In general, the merits of a reconfiguration arrangement concept can be judged on the projected required failure rate of each switch of the arrangement to achieve less than or equal to a certain percentage power loss with a given probability. This indirectly establishes a design philosophy that failure rates of each switch should be inversely proportional to the power that would be lost if that switch were to fail. Each of the configuration concepts investigated has slightly different failure modes which will cause varying amounts of array power capability to be lost with a given switch failure. Also, in each class of reconfiguration arrangements, for a given set of power transfer conditions, various switches can fail and still not constitute a power failure. A trivial example of this would be switches desired ON that fail short and those desired OFF that fail open. Therefore, at this point in the investigation of reconfigurable high voltage solar arrays, qualitative evaluations together with certain numerical bounds appear to present the most fruitful approaches.

A relatively simple model is now considered. Assume that any switch failure will constitute a fractional power loss. Let there be N switches and

let the failure of a switch cause the fraction β/N ($0 \leq \beta \leq N$) of the total array power to be inaccessible to the load. Then the probability that $\beta M/N$ of the total power or less will be lost will be denoted by $R_{C/M}$ where

$$R_{C/M} = \sum_{k=0}^M \binom{N}{k} f_{SW}^k (1 - f_{SW})^{N-k}$$

and f_{SW} is the failure probability of each switch. This is essentially the reliability of the reconfiguration subsystem to successfully transfer at least the fraction $(N - \beta M)/N$ of the total power.

For the reconfiguration arrangement to transfer the total power successfully (except for dissipative losses in the switches) requires that $M = 0$. For this case, the equation is simply

$$R_{C/O} = (1 - f_{SW})^N = R_{SW}^N$$

corresponding to a series string of N switches all of which must operate. For $N f_{SW} \ll 1$

$$R_{C/O} \cong 1 - N f_{SW}$$

and it follows that the projected required switch failure probability of an individual switch should satisfy

$$f_{SW} \leq \frac{1 - R_{C/O}}{N}$$

For 100 switches (considered a reasonable estimate for a versatile arrangement), and for $R_{C/O} = 0.99$, the required value of f_{SW} and R_{SW} becomes

$$f_{SW(100)} \leq 10^{-4}$$

$$R_{SW(100)} \leq 0.9999$$

Total mission time for the suggested mission (orbit raising plus 5 years on station) is approximately 4.5×10^4 hours. If an exponential reliability function is assumed, i. e.,

$$R_{SW} = e^{-\lambda t}$$

where λ is the failure rate in failures/hours, then the requirement becomes

$$\lambda \leq 2.2 \text{ failures}/10^9 \text{ hours.}$$

The typical (operational) nominal failure rates of switchable solid-state devices (power transistors, silicon controlled rectifiers, etc.) operated at 25° C and at 20 percent rated stress would be expected to fall within the range of 50 to 100 failures/ 10^9 hours. It seems reasonable to expect from considerations of the switch model and the environmental extremes, failure rates two orders of magnitude greater than the required 2.2 failures/ 10^9 hours. It then follows that $R_{C/O} \cong 0.368$, a completely unacceptable value.

The switch function reliability, as projected for single element solid-state switches must be improved. Prior to a specific consideration of techniques for improving this reliability, the discussion will return to a further evaluation of $R_{C/M}$. When $N f_{SW}$ is of the order of 1, the following estimate (Poisson's theorem) is valid.

$$R_{C/M} \approx e^{-N f_{SW}} \left(\sum_{k=0}^M \frac{(N f_{SW})^k}{k!} \right)$$

With $N = 100$ and $f_{SW} = 0.01$

$$R_{C/M} \approx 0.368 \sum_{k=0}^M \frac{1}{k!}$$

Then for varying M , approximate values for $R_{C/M}$ are:

M	$R_{C/M}$
0	0.368
1	0.736
2	0.920
3	0.981
4	0.996

This indicates for the model assumed, with a 0.996 probability (100 - 48) percent of the power will be successfully reconfigured. Even for the reconfiguration concept considered, the most promising for low power loss per switch failure, the preassigned array shown in Figure 47 of the main text, the value of β could be 2 or greater, giving a projected gross power loss in excess of 8 percent.

As specified earlier, the values presented are rough estimates using a very simple model. In general, however, as more alternate transfer and routing paths are incorporated in the switching arrangement, the more opportunity there is for power loss, especially when the transfer devices (switches) are anticipated to be less reliable than the power source. When this is true, simple reconfiguration arrangements (using techniques of switch element redundancy) are preferred over the sophisticated, highly flexible arrangements.

Improvement of the Switching Reliability

If the reliability of each reconfiguration switch element is too low to achieve the overall system reliability objectives, certain alternate approaches are possible.

Because of the projected relative weight and size of the switch in comparison to the power controlled by each, some type of switch redundancy will be preferred to providing additional array power to compensate for losses. This observation must be tempered, since certain redundant switch arrangements can lead to increased dissipative switch losses (particularly solid-state devices) which offset the reduction in power losses by switch failures. This tradeoff is beyond the scope of the present study, but certainly must be performed to determine the best approach to improve the reconfiguration reliability of specific configurations when load and switch characteristics are specified.

Often one of the switch failure modes will predominate, leading to the conditions $f_{SWO}/f_{SWS} \gg 1$ or $f_{SWO}/f_{SWS} \ll 1$. In the cases $f_{SW} \approx f_{SWO}$ or $f_{SW} \approx f_{SWS}$, an appropriate parallel or series arrangements of switches can reduce the composite switching function failure probability, possibly two

orders of magnitude or more. With this approach, however, the non-predominant mode failure probability will be increased. If not all switches lead to the same percentage of power loss per switch failure, switch redundancy may be provided for only the critical switches. When $f_{SWO}/f_{SWS} \approx 1$ and $f_{SW} = f_{SWO} + f_{SWS}$ is not acceptable, series-parallel or parallel-series arrangements of switch elements should be considered, i. e., quads. A quad arrangement would reduce the switch failure probability by a factor of 1/67 for $f_{SWS} = f_{SWO}$, $f_{SW} = f_{SWS} + f_{SWO} = 0.01$.

Although the discussion to this point has been sufficiently general to be relevant to any type of switch, some basic remarks should be made concerning mechanical switching devices, particularly high voltage vacuum relays. For such devices, the failure rate is primarily determined by the number of switching operations and not by the length of static operational service. High reliability devices meeting the voltage contact and control isolation requirements presently envisioned should have a representative failure rate of approximately 10^{-3} failures/1000 operations, or a projected failure probability of 10^{-5} for 10 operations. If relays were employed in switch positions which are electrically critical but which require few operations (for major reconfiguration; e. g., the transfer from ion thrusters to communication tubes), an easement of reconfiguration reliability problems is possible.

APPENDIX F. SWITCHING TRANSIENTS ON HIGH VOLTAGE SOLAR ARRAYS CAUSED BY SURFACE CHARGING

If cell blocks on a solar panel are switched from one to another voltage level (with respect to space potential), a change will occur in the state of surface charging of all insulators with which the solar cells are in contact. This change is a result of polarization currents which flow from the environmental plasma to the insulator surfaces until a new equilibrium is reached. Since equal and opposite polarization currents pass through the array circuit, plasma charging is of some consequence to the transient behavior of the array output.

To determine these transients, a solar array with cells which are covered by 0.015 cm (6 mil) quartz slides and backed by a 0.012 cm (5 mil) Kapton layer will be considered (see Figure F-1). Furthermore, it will be assumed that a cell block of 61,600 cells with an end-of-life output of 1 kv and 0.94 ampere is switched from zero to plus 15,000 volts. Since this is the most extreme voltage change on a 16,000 volt array, it gives an upper limit for the anticipated transients. In addition, it will be assumed that the currents drawn from the environmental plasma are given by the product of random plasma current density, j_r , and exposed insulator area, F_N . This implies a relatively small plasma sheath width (see Figure F-1) which, in turn, assumes a relatively high plasma density. It will be seen below that only the case of high plasma density is of significance. Finally, it will be assumed that in equilibrium the insulator surfaces adopt a potential which is very close to space potential. The last two assumptions are based upon results obtained in the High Voltage Solar Array Study (Contract NAS 3-11535) (Reference 1).

The switching transients can be described by the circuit shown in Figure F-2. In the absence of plasma charging (that is in a vacuum environment), cell block "N", which is switched, has the distributed capacity C_N against all other parts of the array and the spacecraft. C_N is assumed to be on the order of $10^{-10}F$. An additional capacity C_{NS} makes itself felt in the presence of a plasma. C_{NS} is given by

$$C_{NS} = \frac{\epsilon_1 \epsilon_0 F_N}{d_1} + \frac{\epsilon_2 \epsilon_0 F_N}{d_2}$$

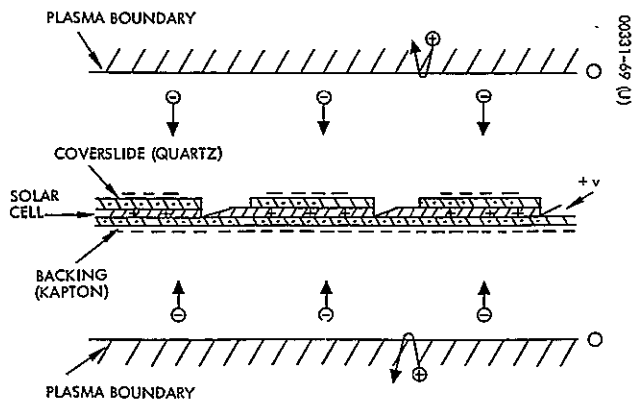


Figure F-1. Solar Array Embedded in Plasma Environment

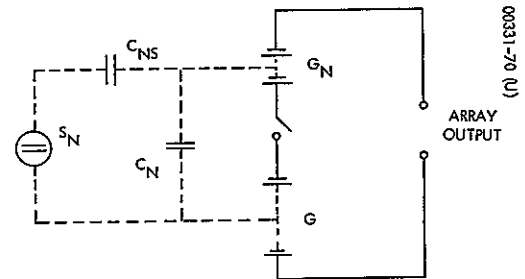


Figure F-2. Equivalent Circuit of Solar Array in Contact With its Plasma Environment

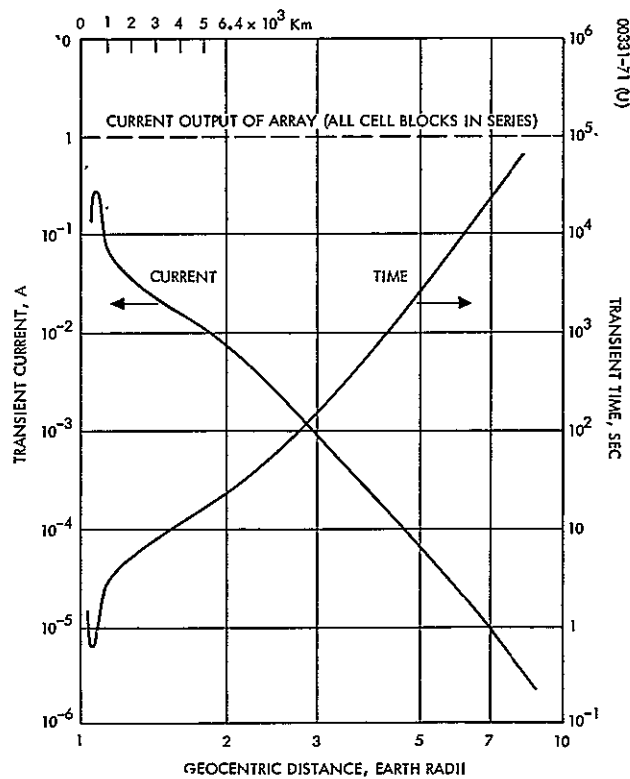


Figure F-3. Magnitude (in Current) and Time Duration of Cellblock Switching Transients on High Voltage Solar Array

where F_N is the cellblock area, ϵ_1 and ϵ_2 are the dielectric constants and d_1 and d_2 are the layer thicknesses of the coverslides and backing. With $F_N = 2.5 \times 10^5 \text{ cm}^2$, $\epsilon_1 = 4$, $\epsilon_2 = 3$, $d_1 = 1.5 \times 10^{-2} \text{ cm}$ and $d_2 = 1.25 \times 10^{-2} \text{ cm}$, C_{NS} becomes about 10^{-5} F . The current-voltage output of the array minus that of the cell block N is represented by a generator G, the output of cellblock N by a generator G_N . Currents arriving from the plasma are considered produced by a constant current source S_N .

The switching sequence can be described as follows: as soon as cellblock N has been connected to the new voltage level, generator G charges capacitor C_N . The charging time is given approximately by

$$\tau_1 = \frac{C_N \Delta V}{I}$$

where ΔV is the change of voltage level of cellblock N, and I is the current output of the array. With $\Delta V = 15,000$ volts and $I = 0.94$ ampere (all cellblocks connected in series), the initial switching transient is on the order of $1.5 \text{ } \mu\text{sec}$.

As soon as C_N starts to charge, generator S_N begins to deliver current to capacitor C_{NS} . The current loop is closed via generator G. Accordingly, part of the current output of the array is used to charge capacitor C_{NS} and is not available at the output terminals. The charging current, I_c , is given by

$$I_c = j_r \cdot F_N$$

where j_r is the plasma random current density (of the particle species which is attracted to the array) and F_N is the cellblock area. With $F_N = 2.5 \times 10^5 \text{ cm}^2$ and $j_r = 10^{-6} \text{ A/cm}^2$ for the densest ionospheric regions (electron density $\cong 10^6 / \text{cm}^3$), one obtains a charging current of 250 ma. This is about a quarter of the array output current and therefore quite significant. At locations in space where the plasma density is lower, the charging current will be correspondingly smaller. Figure F-3 shows the charging current as a function of distance from earth.

The time during which the charging current flows is given by

$$\tau_2 = \frac{C_{NS} \Delta V}{I_c}$$

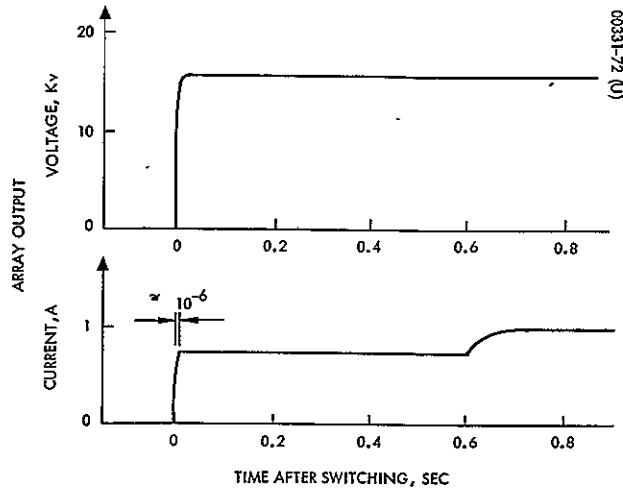


Figure F-4. Time Sequence During Cellblock Switching

For the case of a plasma current of 250 ma, τ_2 becomes 0.6 second. At lower plasma currents, the time becomes larger. Figure F-3 also shows τ_2 as a function of distance from earth. Finally, Figure F-4 gives a time sequence of the output current for the case of a high environmental plasma density and under the simplifying assumption that the array output voltage is kept constant.

CONCLUSION

Cellblock switching on solar arrays can lead to relatively long transients during which the array current output is slightly reduced. The most severe reduction is expected to occur in the densest portions of the ionosphere. There, switching of a cellblock from zero to +15,000 volts will lead to a reduction in the output current by about 25 percent for a period of 0.6 second. In space regions where the plasma density is lower, the current reduction is smaller; however, it lasts longer.

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